

ZC702 EVALUATION PLATFORM HW-Z7-ZC702

(XC7Z020-CLG484)

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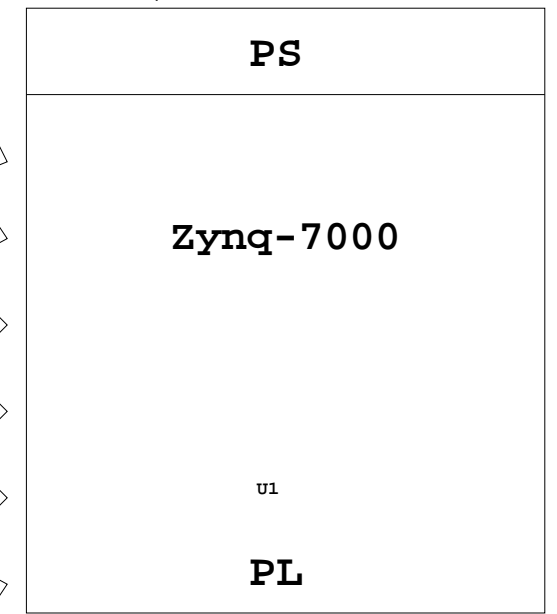
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SCHEM, ROHS COMPLIANT		PCB P/N: 1280617
ZC702 EVALUATION PLATFORM		SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 1 of 48	Drawn By BF	

DDR3 Components
4x256Mx8 SDRAM
Pages 16-19

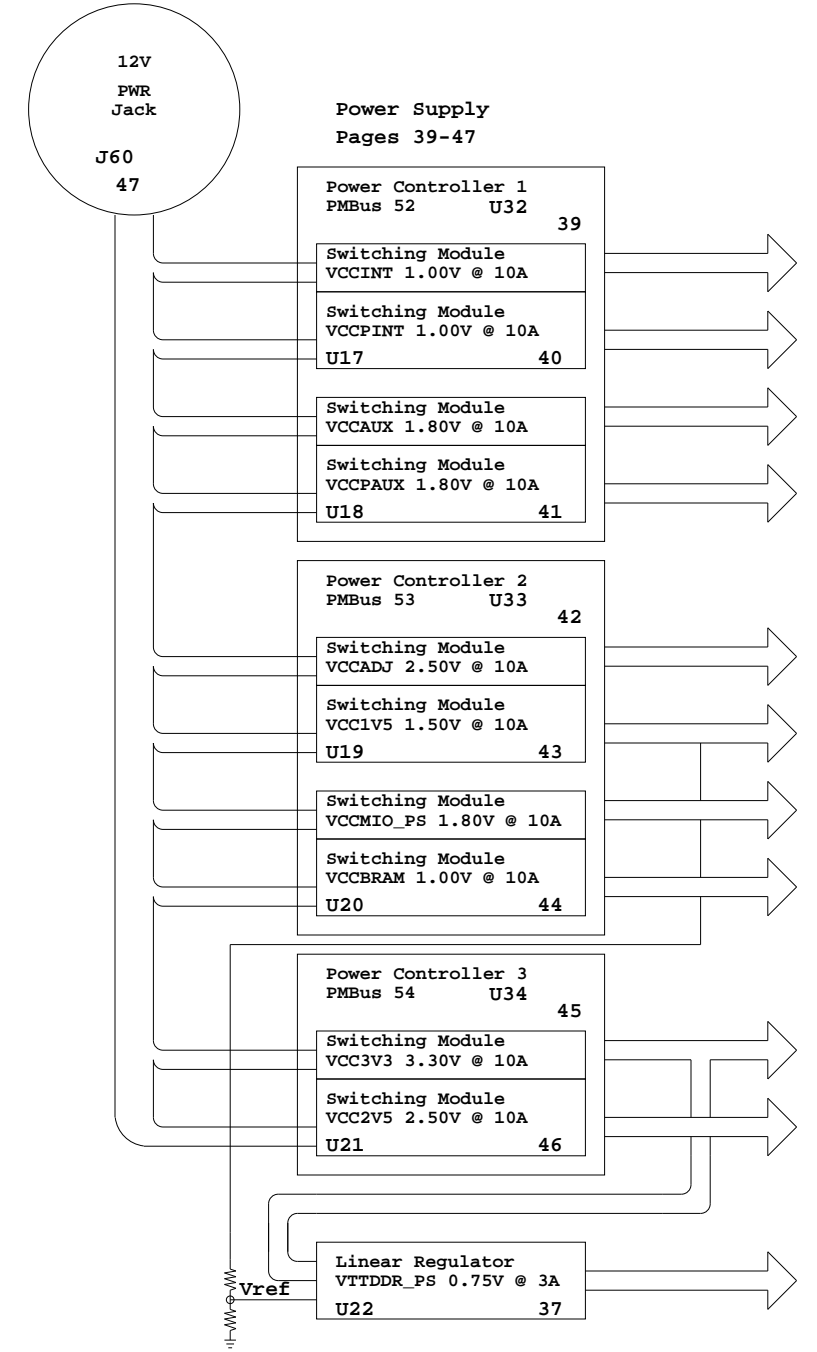
Single Ended Clock
Reset/POR pushbuttons
Page 14



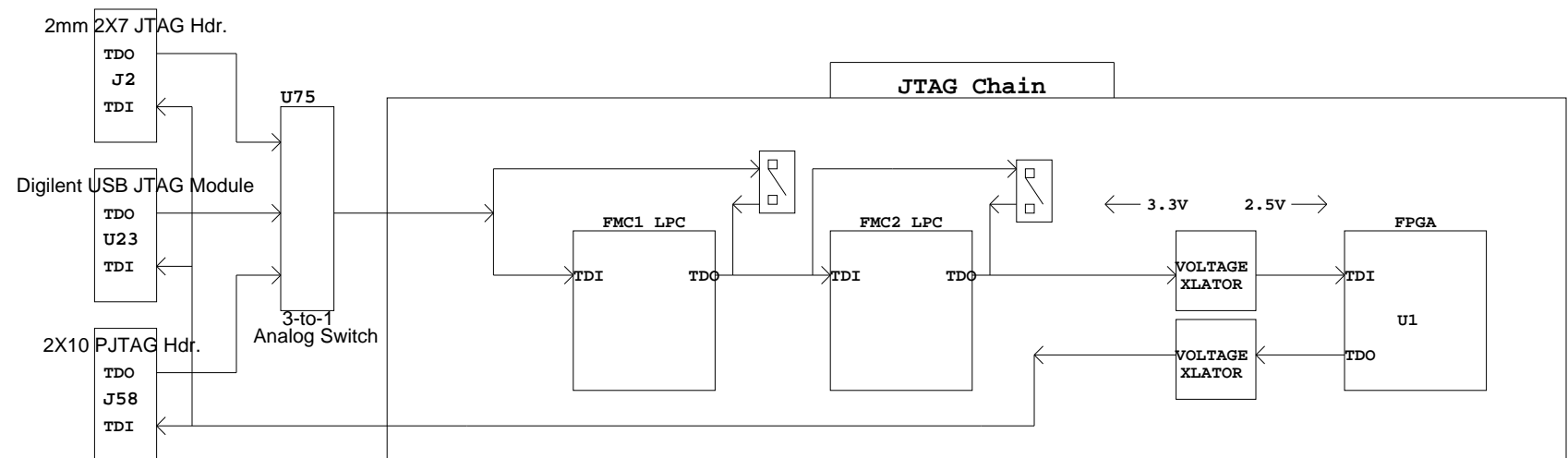
- JTAG Module & Connector
Page 15
- QUAD SPI
Page 20
- CAN Bus
Page 21
- SD Card Connector
Page 22
- FMC1 LPC Connector
Page 23
- FMC2 LPC Connector
Page 24
- 10/100/1000 Ethernet PHY RGMII Only
Pages 26&26

- Trace/Debug Connector
Page 15
- USB UART
Page 36
- ARM PJTAG Hdr.
Page 35
- Switches LEDs, Buttons
Page 34
- IIC RTC
Page 33

- MECHANICALS
Page 38
- USB 2.0 ULPI Xcvr. PHY & Connector
Page 27
- HDMI CODEC & Connector
Pages 28&29
- Configurable Clocks
Page 30
- XADC Hdr.
Page 31
- IIC MUX IIC EEPROM
Page 32



IIC Addressing	
0b1110100	PCA9548
0b1011101	SI570
0bxxxxxx00	FMC LPC 1
0bxxxxxx00	FMC LPC 2
0b1010100	IIC EEPROM
0b0100001	IIC Port Expander
0b0111001	ADV7512
0b1010010 0b1010011 0b1010100	PMBUS Controllers



IRONWOOD FFG1761 SOCKET
SUPPORTS MULTIPLE DEVICES
REFER TO BOARD BILL OF MATERIALS ON XILINX.COM
TO CONFIRM FPGA PROVIDED

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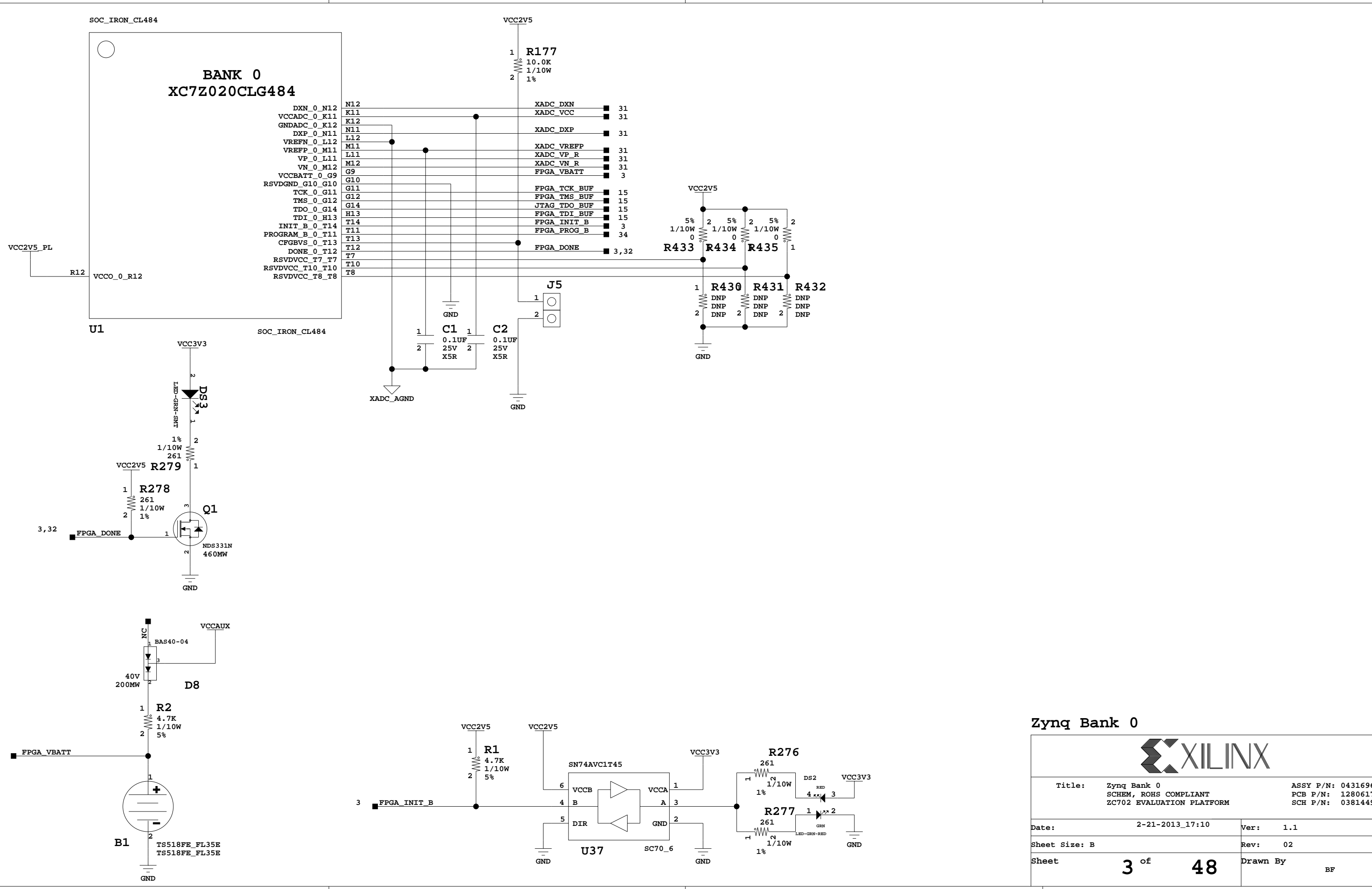
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Title: ZC702 Block Diagram SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM

Date: 2-21-2013_17:10 Ver: 1.1

Sheet Size: B Rev: 02

Sheet **2** of **48** Drawn By BF



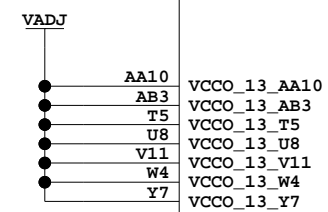
Zynq Bank 0



Title: Zynq Bank 0 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 3 of 48	Drawn By BF	

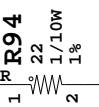
SOC_IRON_CL484

BANK 13 XC7Z020CLG484



IO_0_13_R7	R7
IO_L1P_T0_13_V10	V10
IO_L1N_T0_13_V9	V9
IO_L2P_T0_13_V8	V8
IO_L2N_T0_13_W8	W8
IO_L3P_T0_DQS_13_W11	W11
IO_L3N_T0_DQS_13_W10	W10
IO_L4P_T0_13_V12	V12
IO_L4N_T0_13_W12	W12
IO_L5P_T0_13_U12	U12
IO_L5N_T0_13_U11	U11
IO_L6P_T0_13_U10	U10
IO_L6N_T0_VREF_13_U9	U9
IO_L7P_T1_13_AA12	AA12
IO_L7N_T1_13_AB12	AB12
IO_L8P_T1_13_AA11	AA11
IO_L8N_T1_13_AB11	AB11
IO_L9P_T1_DQS_13_AB10	AB10
IO_L9N_T1_DQS_13_AB9	AB9
IO_L10P_T1_13_Y11	Y11
IO_L10N_T1_13_Y10	Y10
IO_L11P_T1_SRCC_13_AA9	AA9
IO_L11N_T1_SRCC_13_AA8	AA8
IO_L12P_T1_MRCC_13_Y9	Y9
IO_L12N_T1_MRCC_13_Y8	Y8
IO_L13P_T2_MRCC_13_Y6	Y6
IO_L13N_T2_MRCC_13_Y5	Y5
IO_L14P_T2_SRCC_13_AA7	AA7
IO_L14N_T2_SRCC_13_AA6	AA6
IO_L15P_T2_DQS_13_AB2	AB2
IO_L15N_T2_DQS_13_AB1	AB1
IO_L16P_T2_13_AB5	AB5
IO_L16N_T2_13_AB4	AB4
IO_L17P_T2_13_AB7	AB7
IO_L17N_T2_13_AB6	AB6
IO_L18P_T2_13_Y4	Y4
IO_L18N_T2_13_AA4	AA4
IO_L19P_T3_13_R6	R6
IO_L19N_T3_VREF_13_T6	T6
IO_L20P_T3_13_T4	T4
IO_L20N_T3_13_U4	U4
IO_L21P_T3_DQS_13_V5	V5
IO_L21N_T3_DQS_13_V4	V4
IO_L22P_T3_13_U6	U6
IO_L22N_T3_13_U5	U5
IO_L23P_T3_13_V7	V7
IO_L23N_T3_13_W7	W7
IO_L24P_T3_13_W6	W6
IO_L24N_T3_13_W5	W5
IO_25_13_U7	U7

PL_PJTAG_TDO	R	35
PL_PJTAG_TCK	R	35
PL_PJTAG_TMS	R	35
PL_PJTAG_TDI	R	35
IIC_SDA_MAIN_LS	R	32
IIC_SCL_MAIN_LS	R	32
PMOD2_1_LS	R	34
FMC2_LPC_LA23_P	R	24
FMC2_LPC_LA23_N	R	24
FMC2_LPC_LA26_P	R	24
FMC2_LPC_LA26_N	R	24
FMC2_LPC_LA22_P	R	24
FMC2_LPC_LA22_N	R	24
FMC2_LPC_LA25_P	R	24
FMC2_LPC_LA25_N	R	24
FMC2_LPC_LA29_P	R	24
FMC2_LPC_LA29_N	R	24
FMC2_LPC_LA31_P	R	24
FMC2_LPC_LA31_N	R	24
FMC2_LPC_LA33_P	R	24
FMC2_LPC_LA33_N	R	24
FMC2_LPC_LA18_CC_P	R	24
FMC2_LPC_LA18_CC_N	R	24
USRCLK_P	R	30
USRCLK_N	R	30
FMC2_LPC_CLK1_M2C_P	R	24
FMC2_LPC_CLK1_M2C_N	R	24
FMC2_LPC_LA17_CC_P	R	24
FMC2_LPC_LA17_CC_N	R	24
FMC2_LPC_LA27_P	R	24
FMC2_LPC_LA27_N	R	24
FMC2_LPC_LA28_P	R	24
FMC2_LPC_LA28_N	R	24
FMC2_LPC_LA30_P	R	24
FMC2_LPC_LA30_N	R	24
FMC2_LPC_LA32_P	R	24
FMC2_LPC_LA32_N	R	24
FMC2_LPC_LA19_P	R	24
FMC2_LPC_LA19_N	R	24
FMC2_LPC_LA20_P	R	24
FMC2_LPC_LA20_N	R	24
FMC2_LPC_LA21_P	R	24
FMC2_LPC_LA21_N	R	24
FMC2_LPC_LA24_P	R	24
FMC2_LPC_LA24_N	R	24
PMOD2_0_LS	R	34
GPIO_DIP_SW1	R	34
GPIO_DIP_SW0	R	34
PMOD1_3_LS	R	35
IIC_RTC_IRQ_1_B	R	33



U1

SOC_IRON_CL484

Zynq Bank 13



Title: Zynq Bank 13 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 4 of 48	Drawn By BF	

SOC_IRON_CL484

BANK 33 XC7Z020CLG484

VADJ

AA20	VCCO_33_AA20
AB13	VCCO_33_AB13
U18	VCCO_33_U18
V21	VCCO_33_V21
W14	VCCO_33_W14
Y17	VCCO_33_Y17

IO_0_33_U19	U19	HDMI_R_D12	29
IO_L1P_T0_33_T21	T21	FMC2_LPC_LA07_P	24
IO_L1N_T0_33_U21	U21	FMC2_LPC_LA07_N	24
IO_L2P_T0_33_T22	T22	FMC2_LPC_LA14_P	24
IO_L2N_T0_33_U22	U22	FMC2_LPC_LA14_N	24
IO_L3P_T0_DQS_33_V22	V22	FMC2_LPC_LA13_P	24
IO_L3N_T0_DQS_33_W22	W22	FMC2_LPC_LA13_N	24
IO_L4P_T0_33_W20	W20	HDMI_R_D9	29
IO_L4N_T0_33_W21	W21	HDMI_R_D8	29
IO_L5P_T0_33_U20	U20	HDMI_R_D7	29
IO_L5N_T0_33_V20	V20	HDMI_R_D6	29
IO_L6P_T0_33_V18	V18	HDMI_R_D5	29
IO_L6N_T0_VREF_33_V19	V19	HDMI_R_D4	29
IO_L7P_T1_33_AA22	AA22	HDMI_R_D3	29
IO_L7N_T1_33_AB22	AB22	HDMI_R_D2	29
IO_L8P_T1_33_AA21	AA21	HDMI_R_D1	29
IO_L8N_T1_33_AB21	AB21	HDMI_R_D0	29
IO_L9P_T1_DQS_33_Y20	Y20	FMC2_LPC_LA10_P	24
IO_L9N_T1_DQS_33_Y21	Y21	FMC2_LPC_LA10_N	24
IO_L10P_T1_33_AB19	AB19	FMC2_LPC_LA05_P	24
IO_L10N_T1_33_AB20	AB20	FMC2_LPC_LA05_N	24
IO_L11P_T1_SRCC_33_Y19	Y19	FMC2_LPC_LA00_CC_P	24
IO_L11N_T1_SRCC_33_AA19	AA19	FMC2_LPC_LA00_CC_N	24
IO_L12P_T1_MRCC_33_Y18	Y18	FMC2_LPC_CLK0_M2C_P	24
IO_L12N_T1_MRCC_33_AA18	AA18	FMC2_LPC_CLK0_M2C_N	24
IO_L13P_T2_MRCC_33_W17	W17	PMOD1_2_LS	35
IO_L13N_T2_MRCC_33_W18	W18	HDMI_R_D10	29
IO_L14P_T2_SRCC_33_W16	W16	FMC2_LPC_LA01_CC_P	24
IO_L14N_T2_SRCC_33_Y16	Y16	FMC2_LPC_LA01_CC_N	24
IO_L15P_T2_DQS_33_U15	U15	FMC2_LPC_LA09_P	24
IO_L15N_T2_DQS_33_U16	U16	FMC2_LPC_LA09_N	24
IO_L16P_T2_33_U17	U17	FMC2_LPC_LA06_P	24
IO_L16N_T2_33_V17	V17	FMC2_LPC_LA06_N	24
IO_L17P_T2_33_AA17	AA17	FMC2_LPC_LA08_P	24
IO_L17N_T2_33_AB17	AB17	FMC2_LPC_LA08_N	24
IO_L18P_T2_33_AA16	AA16	FMC2_LPC_LA03_P	24
IO_L18N_T2_33_AB16	AB16	FMC2_LPC_LA03_N	24
IO_L19P_T3_33_V14	V14	FMC2_LPC_LA02_P	24
IO_L19N_T3_VREF_33_V15	V15	FMC2_LPC_LA02_N	24
IO_L20P_T3_33_V13	V13	FMC2_LPC_LA04_P	24
IO_L20N_T3_33_W13	W13	FMC2_LPC_LA04_N	24
IO_L21P_T3_DQS_33_W15	W15	FMC2_LPC_LA12_P	24
IO_L21N_T3_DQS_33_Y15	Y15	FMC2_LPC_LA12_N	24
IO_L22P_T3_33_Y14	Y14	FMC2_LPC_LA11_P	24
IO_L22N_T3_33_AA14	AA14	FMC2_LPC_LA11_N	24
IO_L23P_T3_33_Y13	Y13	FMC2_LPC_LA15_P	24
IO_L23N_T3_33_AA13	AA13	FMC2_LPC_LA15_N	24
IO_L24P_T3_33_AB14	AB14	FMC2_LPC_LA16_P	24
IO_L24N_T3_33_AB15	AB15	FMC2_LPC_LA16_N	24
IO_25_33_U14	U14	HDMI_INT	28

U1

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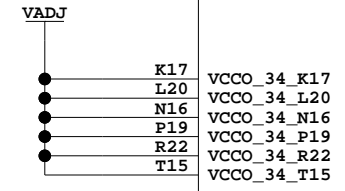
Zynq Bank 33



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Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 5 of 48	Drawn By BF	

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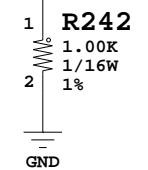
BANK 34 XC7Z020CLG484



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IO_0_34_H15	H15	HDMI R VSYNC	29
IO_L1P_T0_34_J15	J15	FMCI LPC LA07 P	23
IO_L1N_T0_34_K15	K15	FMCI LPC LA07 N	23
IO_L2P_T0_34_J16	J16	FMCI LPC LA14 P	23
IO_L2N_T0_34_J17	J17	FMCI LPC LA14 N	23
IO_L3P_T0_DQS_PUDC_B_34_K16	K16		
IO_L3N_T0_DQS_34_L16	L16	HDMI R CLK	29
IO_L4P_T0_34_L17	L17	FMCI LPC LA10 P	23
IO_L4N_T0_34_M17	M17	FMCI LPC LA10 N	23
IO_L5P_T0_34_N17	N17	FMCI LPC LA05 P	23
IO_L5N_T0_34_N18	N18	FMCI LPC LA05 N	23
IO_L6P_T0_34_M15	M15	FMCI LPC LA09 P	23
IO_L6N_T0_VREF_34_M16	M16	FMCI LPC LA09 N	23
IO_L7P_T1_34_J18	J18	FMCI LPC LA06 P	23
IO_L7N_T1_34_K18	K18	FMCI LPC LA06 N	23
IO_L8P_T1_34_J21	J21	FMCI LPC LA08 P	23
IO_L8N_T1_34_J22	J22	FMCI LPC LA08 N	23
IO_L9P_T1_DQS_34_J20	J20	FMCI LPC LA03 P	23
IO_L9N_T1_DQS_34_K21	K21	FMCI LPC LA03 N	23
IO_L10P_T1_34_L21	L21	FMCI LPC LA02 P	23
IO_L10N_T1_34_L22	L22	FMCI LPC LA02 N	23
IO_L11P_T1_SRCC_34_K19	K19	FMCI LPC LA00 CC P	23
IO_L11N_T1_SRCC_34_K20	K20	FMCI LPC LA00 CC N	23
IO_L12P_T1_MRCC_34_L18	L18	FMCI LPC CLK0 M2C P	23
IO_L12N_T1_MRCC_34_L19	L19	FMCI LPC CLK0 M2C N	23
IO_L13P_T2_MRCC_34_M19	M19	FMCI LPC CLK1 M2C P	23
IO_L13N_T2_MRCC_34_M20	M20	FMCI LPC CLK1 M2C N	23
IO_L14P_T2_SRCC_34_N19	N19	FMCI LPC LA01 CC P	23
IO_L14N_T2_SRCC_34_N20	N20	FMCI LPC LA01 CC N	23
IO_L15P_T2_DQS_34_M21	M21	FMCI LPC LA04 P	23
IO_L15N_T2_DQS_34_M22	M22	FMCI LPC LA04 N	23
IO_L16P_T2_34_N22	N22	FMCI LPC LA12 P	23
IO_L16N_T2_34_P22	P22	FMCI LPC LA12 N	23
IO_L17P_T2_34_R20	R20	FMCI LPC LA11 P	23
IO_L17N_T2_34_R21	R21	FMCI LPC LA11 N	23
IO_L18P_T2_34_P20	P20	FMCI LPC LA15 P	23
IO_L18N_T2_34_P21	P21	FMCI LPC LA15 N	23
IO_L19P_T3_34_N15	N15	FMCI LPC LA16 P	23
IO_L19N_T3_VREF_34_P15	P15	FMCI LPC LA16 N	23
IO_L20P_T3_34_P17	P17	PMOD2 3 LS	34
IO_L20N_T3_34_P18	P18	PMOD2 2 LS	34
IO_L21P_T3_DQS_34_T16	T16	HDMI R D15	29
IO_L21N_T3_DQS_34_T17	T17	HDMI R D14	29
IO_L22P_T3_34_R19	R19	HDMI R D13	29
IO_L22N_T3_34_T19	T19	HDMI R D11	29
IO_L23P_T3_34_R18	R18	HDMI R HSYNC	29
IO_L23N_T3_34_T18	T18	HDMI R DE	29
IO_L24P_T3_34_P16	P16	FMCI LPC LA13 P	23
IO_L24N_T3_34_R16	R16	FMCI LPC LA13 N	23
IO_25_34_R15	R15	HDMI R SPDIF	29



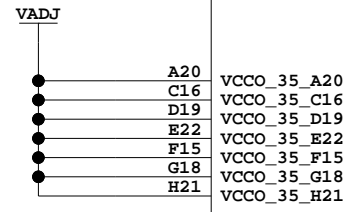
Zynq Bank 34



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Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 6 of 48	Drawn By BF	

SOC_IRON_CL484

BANK 35 XC7Z020CLG484



IO_0_35_H17	H17	XADC_GPIO_0	31
IO_L1P_T0_AD0P_35_F16	F16	XADC_VAUX0P_R	31
IO_L1N_T0_AD0N_35_E16	E16	XADC_VAUX0N_R	31
IO_L2P_T0_AD8P_35_D16	D16	XADC_VAUX8P_R	31
IO_L2N_T0_AD8N_35_D17	D17	XADC_VAUX8N_R	31
IO_L3P_T0_DQS_AD1P_35_E15	E15	PMOD1_0_LS	35
IO_L3N_T0_DQS_AD1N_35_D15	D15	PMOD1_1_LS	35
IO_L4P_T0_35_G15	G15	FMCI_LPC_LA23_P	23
IO_L4N_T0_35_G16	G16	FMCI_LPC_LA23_N	23
IO_L5P_T0_AD9P_35_F18	F18	FMCI_LPC_LA26_P	23
IO_L5N_T0_AD9N_35_E18	E18	FMCI_LPC_LA26_N	23
IO_L6P_T0_35_G17	G17	FMCI_LPC_LA22_P	23
IO_L6N_T0_VREF_35_F17	F17	FMCI_LPC_LA22_N	23
IO_L7P_T1_AD2P_35_C15	C15	FMCI_LPC_LA25_P	23
IO_L7N_T1_AD2N_35_B15	B15	FMCI_LPC_LA25_N	23
IO_L8P_T1_AD10P_35_B16	B16	FMCI_LPC_LA29_P	23
IO_L8N_T1_AD10N_35_B17	B17	FMCI_LPC_LA29_N	23
IO_L9P_T1_DQS_AD3P_35_A16	A16	FMCI_LPC_LA31_P	23
IO_L9N_T1_DQS_AD3N_35_A17	A17	FMCI_LPC_LA31_N	23
IO_L10P_T1_AD11P_35_A18	A18	FMCI_LPC_LA33_P	23
IO_L10N_T1_AD11N_35_A19	A19	FMCI_LPC_LA33_N	23
IO_L11P_T1_SRCC_35_C17	C17	FMCI_LPC_LA27_P	23
IO_L11N_T1_SRCC_35_C18	C18	FMCI_LPC_LA27_N	23
IO_L12P_T1_MRCC_35_D18	D18	SYSCLK_P	30
IO_L12N_T1_MRCC_35_C19	C19	SYSCLK_N	30
IO_L13P_T2_MRCC_35_B19	B19	FMCI_LPC_LA17_CC_P	23
IO_L13N_T2_MRCC_35_B20	B20	FMCI_LPC_LA17_CC_N	23
IO_L14P_T2_AD4P_SRCC_35_D20	D20	FMCI_LPC_LA18_CC_P	23
IO_L14N_T2_AD4N_SRCC_35_C20	C20	FMCI_LPC_LA18_CC_N	23
IO_L15P_T2_DQS_AD12P_35_A21	A21	FMCI_LPC_LA24_P	23
IO_L15N_T2_DQS_AD12N_35_A22	A22	FMCI_LPC_LA24_N	23
IO_L16P_T2_35_D22	D22	FMCI_LPC_LA28_P	23
IO_L16N_T2_35_C22	C22	FMCI_LPC_LA28_N	23
IO_L17P_T2_AD5P_35_E21	E21	FMCI_LPC_LA30_P	23
IO_L17N_T2_AD5N_35_D21	D21	FMCI_LPC_LA30_N	23
IO_L18P_T2_AD13P_35_B21	B21	FMCI_LPC_LA32_P	23
IO_L18N_T2_AD13N_35_B22	B22	FMCI_LPC_LA32_N	23
IO_L19P_T3_35_H19	H19	PWRCTL2_VCC4A_PG_L	23, 24, 42
IO_L19N_T3_VREF_35_H20	H20	HDMI_SPDIF_OUT_LS	34
IO_L20P_T3_AD6P_35_G19	G19	GPIO_SW_N	34
IO_L20N_T3_AD6N_35_F19	F19	GPIO_SW_S	34
IO_L21P_T3_DQS_AD14P_35_E19	E19	FMCI_LPC_LA19_P	23
IO_L21N_T3_DQS_AD14N_35_E20	E20	FMCI_LPC_LA19_N	23
IO_L22P_T3_AD7P_35_G20	G20	FMCI_LPC_LA20_P	23
IO_L22N_T3_AD7N_35_G21	G21	FMCI_LPC_LA20_N	23
IO_L23P_T3_35_F21	F21	FMCI_LPC_LA21_P	23
IO_L23N_T3_35_F22	F22	FMCI_LPC_LA21_N	23
IO_L24P_T3_AD15P_35_H22	H22	XADC_GPIO_1	31
IO_L24N_T3_AD15N_35_G22	G22	XADC_GPIO_2	31
IO_25_35_H18	H18	XADC_GPIO_3	31

U1

SOC_IRON_CL484

Zynq Bank 35

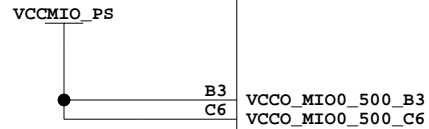


Title: Zynq Bank 35 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 7 of 48	Drawn By BF	

SOC_IRON_CL484

BANK 500 XC7Z020CLG484

PS_CLK_500_F7	F7	PS_CLK	30
PS_POR_B_500_B5	B5	PS_POR_B	14, 25, 27
PS_MIO15_500_E6	E6	SDIO_SDWP	22
PS_MIO14_500_B6	B6	PS_DIP_SW0	8
PS_MIO13_500_A6	A6	IIC_MUX_RESET_B_LS	8
PS_MIO12_500_C5	C5	PS_DIP_SW1	34
PS_MIO11_500_B4	B4	PHY_RESET_B_AND	8
PS_MIO10_500_G7	G7	PS_LED1	25
PS_MIO9_500_C4	C4	CAN_STB_B_LS	8
PS_MIO8_500_E5	E5	PS_MIO8_LED0	21
PS_MIO7_500_D5	D5	USB_RESET_B_AND	8, 14
PS_MIO6_500_A4	A4	QSPI_CLK	14, 27
PS_MIO5_500_A3	A3	QSPI_IO3	14, 20
PS_MIO4_500_E4	E4	QSPI_IO2	14, 20
PS_MIO3_500_F6	F6	QSPI_IO1	14, 20
PS_MIO2_500_A2	A2	QSPI_IO0	14, 20
PS_MIO1_500_A1	A1	QSPI_CS_B	14, 20
PS_MIO0_500_G6	G6	SDIO_SDDT	20
			22



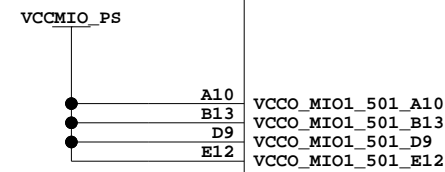
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SOC_IRON_CL484

SOC_IRON_CL484

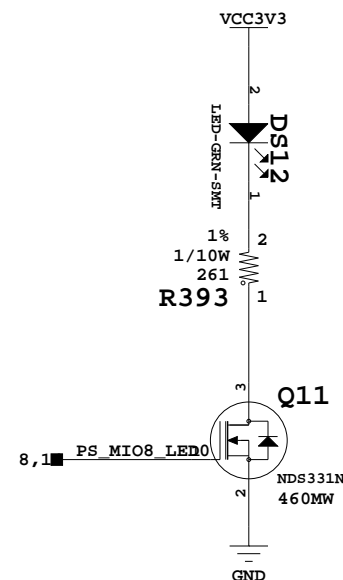
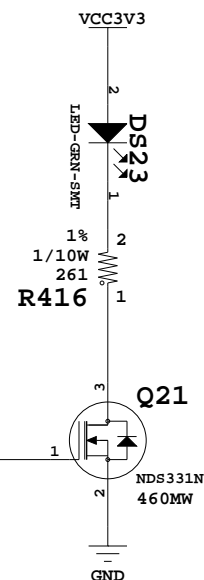
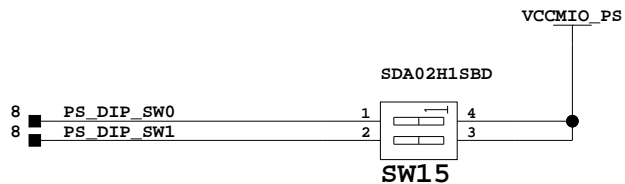
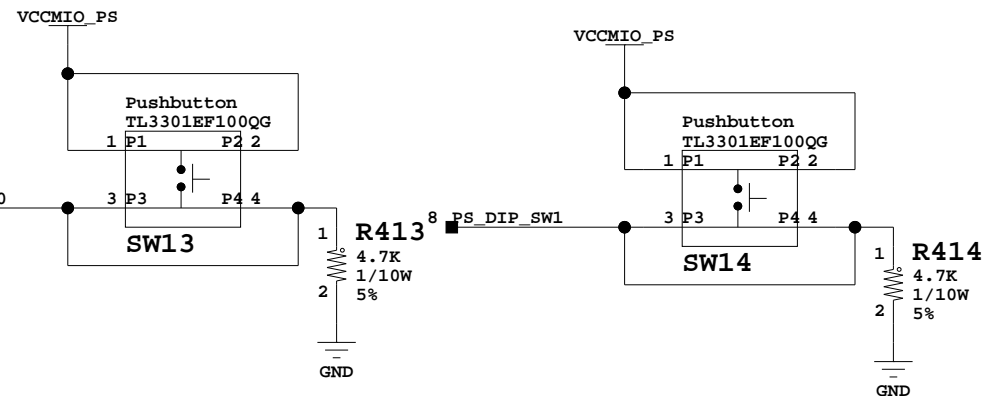
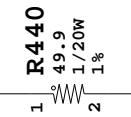
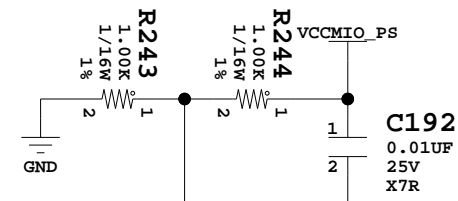
BANK 501 XC7Z020CLG484

PS_MIO_VREF_501_F8	F8	PHY_TXD0	25
PS_MIO17_501_E9	E9	PHY_TXD2	25
PS_MIO19_501_E10	E10	PHY_TX_CTRL	25
PS_MIO21_501_F11	F11	PHY_RXD0	25
PS_MIO23_501_E11	E11	PHY_RXD2	25
PS_MIO25_501_F12	F12	PHY_RX_CTRL	25
PS_MIO27_501_D7	D7	USB_DIR	27
PS_MIO29_501_E8	E8	USB_NXT	27
PS_MIO31_501_F9	F9	USB_DATA1	27
PS_MIO33_501_G13	G13	USB_DATA3	27
PS_MIO35_501_F14	F14	USB_DATA5	27
PS_MIO38_501_F13	F13	USB_DATA6	27
PS_MIO40_501_E14	E14	SDIO_CLK_LS_R	27
PS_MIO42_501_D8	D8	SDIO_DAT0_LS	22
PS_MIO44_501_E13	E13	SDIO_DAT2_LS	22
PS_MIO46_501_D12	D12	CAN_RXD_LS	21
PS_MIO48_501_D11	D11	USB_UART_RX	36
PS_MIO50_501_D13	D13	PS_SCL_MAIN	32
PS_MIO52_501_D10	D10	PHY_MDC	25
PS_SRST_B_501_C9	C9	PS_SRST_B	14
PS_MIO16_501_D6	D6	PHY_TX_CLK	25
PS_MIO18_501_A7	A7	PHY_TXD1	25
PS_MIO20_501_A8	A8	PHY_TXD3	25
PS_MIO22_501_A14	A14	PHY_RX_CLK	25
PS_MIO24_501_B7	B7	PHY_RXD1	25
PS_MIO26_501_A13	A13	PHY_RXD3	25
PS_MIO28_501_A12	A12	USB_DATA4	27
PS_MIO30_501_A11	A11	USB_STP	27
PS_MIO32_501_C7	C7	USB_DATA0	27
PS_MIO34_501_B12	B12	USB_DATA2	27
PS_MIO36_501_A9	A9	USB_CLKOUT	27
PS_MIO37_501_B14	B14	USB_DATA5	27
PS_MIO39_501_C13	C13	USB_DATA7	27
PS_MIO41_501_C8	C8	SDIO_CMD_LS	22
PS_MIO43_501_B11	B11	SDIO_DAT1_LS	22
PS_MIO45_501_B9	B9	SDIO_CD_DAT3_LS	22
PS_MIO47_501_B10	B10	CAN_TXD_LS	21
PS_MIO49_501_C14	C14	USB_UART_TX	36
PS_MIO51_501_C10	C10	PS_SDA_MAIN	32
PS_MIO53_501_C12	C12	PHY_MDIO	32



U1

SOC_IRON_CL484



Zynq Banks 500, 501



Title: Zynq Banks 500, 501
SCHEM, ROHS COMPLIANT
ZC702 EVALUATION PLATFORM

ASSY P/N: 0431696
PCB P/N: 1280617
SCH P/N: 0381449

Date:	2-21-2013_17:10	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	8 of 48	Drawn By	BF

SOC_IRON_CL484

BANK 502 XC7Z020CLG484

PS_DDR_DRST_B_502_F3	F3	PS_DDR3_RESET_B	16,17,18,19
PS_DDR_DQ0_502_D1	D1	PS_DDR3_DQ3	16
PS_DDR_DQ1_502_C3	C3	PS_DDR3_DQ1	16
PS_DDR_DQ2_502_B2	B2	PS_DDR3_DQ6	16
PS_DDR_DQ3_502_D3	D3	PS_DDR3_DQ7	16
PS_DDR_DM0_502_B1	B1	PS_DDR3_DM0	16
PS_DDR_DQS_P0_502_C2	C2	PS_DDR3_DQS0_P	16
PS_DDR_DQS_N0_502_D2	D2	PS_DDR3_DQS0_N	16
PS_DDR_DQ4_502_E3	E3	PS_DDR3_DQ0	16
PS_DDR_DQ5_502_E1	E1	PS_DDR3_DQ5	16
PS_DDR_DQ6_502_F2	F2	PS_DDR3_DQ2	16
PS_DDR_DQ7_502_F1	F1	PS_DDR3_DQ4	16
PS_DDR_DQ8_502_G2	G2	PS_DDR3_DQ8	16
PS_DDR_DQ9_502_G1	G1	PS_DDR3_DQ10	17
PS_DDR_DQ10_502_L1	L1	PS_DDR3_DQ9	17
PS_DDR_DQ11_502_L2	L2	PS_DDR3_DQ13	17
PS_DDR_DM1_502_H3	H3	PS_DDR3_DM1	17
PS_DDR_DQS_P1_502_H2	H2	PS_DDR3_DQS1_P	17
PS_DDR_DQS_N1_502_J2	J2	PS_DDR3_DQS1_N	17
PS_DDR_DQ12_502_L3	L3	PS_DDR3_DQ12	17
PS_DDR_DQ13_502_K1	K1	PS_DDR3_DQ11	17
PS_DDR_DQ14_502_J1	J1	PS_DDR3_DQ14	17
PS_DDR_DQ15_502_K3	K3	PS_DDR3_DQ15	17
PS_DDR_A14_502_G4	G4	PS_DDR3_A14	17,18,19
PS_DDR_A13_502_F4	F4	PS_DDR3_A13	17,18,19
PS_DDR_A12_502_H4	H4	PS_DDR3_A12	17,18,19
PS_DDR_A11_502_G5	G5	PS_DDR3_A11	17,18,19
PS_DDR_A10_502_J3	J3	PS_DDR3_A10	17,18,19
PS_DDR_A9_502_H5	H5	PS_DDR3_A9	17,18,19
PS_DDR_A8_502_J5	J5	PS_DDR3_A8	17,18,19
PS_DDR_A7_502_J6	J6	PS_DDR3_A7	17,18,19
PS_DDR_A6_502_J7	J7	PS_DDR3_A6	17,18,19
PS_DDR_A5_502_K5	K5	PS_DDR3_A5	17,18,19
PS_DDR_A4_502_K6	K6	PS_DDR3_A4	17,18,19
PS_DDR_A3_502_L4	L4	PS_DDR3_A3	17,18,19
PS_DDR_VRN_502_M7	M7	PS_VRN	9
PS_DDR_VRP_502_N7	N7	PS_VRP	9
PS_DDR_CKP_502_N4	N4	PS_DDR3_CLK_P	9
PS_DDR_CKN_502_N5	N5	PS_DDR3_CLK_N	17,18,19
PS_DDR_A2_502_K4	K4	PS_DDR3_A2	17,18,19
PS_DDR_A1_502_M5	M5	PS_DDR3_A1	17,18,19
PS_DDR_A0_502_M4	M4	PS_DDR3_A0	17,18,19
PS_DDR_BA2_502_M6	M6	PS_DDR3_BA2	17,18,19
PS_DDR_BA1_502_L6	L6	PS_DDR3_BA1	17,18,19
PS_DDR_BA0_502_L7	L7	PS_DDR3_BA0	17,18,19
PS_DDR_ODT_502_P5	P5	PS_DDR3_ODT	16,17,18,19
PS_DDR_CS_B_502_P6	P6	PS_DDR3_CS_B	16,17,18,19
PS_DDR_CKE_502_V3	V3	PS_DDR3_CKE	16,17,18,19
PS_DDR_WE_B_502_R4	R4	PS_DDR3_WE_B	16,17,18,19
PS_DDR_CAS_B_502_P3	P3	PS_DDR3_CAS_B	16,17,18,19
PS_DDR_RAS_B_502_R5	R5	PS_DDR3_RAS_B	16,17,18,19
PS_DDR_DQ16_502_M1	M1	PS_DDR3_DQ16	18
PS_DDR_DQ17_502_T3	T3	PS_DDR3_DQ17	18
PS_DDR_DQ18_502_N3	N3	PS_DDR3_DQ18	18
PS_DDR_DQ19_502_T1	T1	PS_DDR3_DQ19	18
PS_DDR_DM2_502_P1	P1	PS_DDR3_DM2	18
PS_DDR_DQS_P2_502_N2	N2	PS_DDR3_DQS2_P	18
PS_DDR_DQS_N2_502_P2	P2	PS_DDR3_DQS2_N	18
PS_DDR_DQ20_502_R3	R3	PS_DDR3_DQ20	18
PS_DDR_DQ21_502_T2	T2	PS_DDR3_DQ21	18
PS_DDR_DQ22_502_M2	M2	PS_DDR3_DQ22	18
PS_DDR_DQ23_502_R1	R1	PS_DDR3_DQ23	18
PS_DDR_DQ24_502_AA3	AA3	PS_DDR3_DQ27	19
PS_DDR_DQ25_502_U1	U1	PS_DDR3_DQ24	19
PS_DDR_DQ26_502_AA1	AA1	PS_DDR3_DQ25	19
PS_DDR_DQ27_502_U2	U2	PS_DDR3_DQ26	19
PS_DDR_DM3_502_AA2	AA2	PS_DDR3_DM3	19
PS_DDR_DQS_P3_502_V2	V2	PS_DDR3_DQS3_P	19
PS_DDR_DQS_N3_502_W2	W2	PS_DDR3_DQS3_N	19
PS_DDR_DQ28_502_W1	W1	PS_DDR3_DQ28	19
PS_DDR_DQ29_502_Y3	Y3	PS_DDR3_DQ29	19
PS_DDR_DQ30_502_W3	W3	PS_DDR3_DQ30	19
PS_DDR_DQ31_502_Y1	Y1	PS_DDR3_DQ31	19
PS_DDR_VREF0_502_H7	H7		
PS_DDR_VREF1_502_P7	P7		

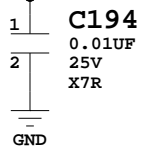
VCC1V5_PS

E2	VCCO_DDR_502_E2
F5	VCCO_DDR_502_F5
H1	VCCO_DDR_502_H1
J4	VCCO_DDR_502_J4
K7	VCCO_DDR_502_K7
M3	VCCO_DDR_502_M3
N6	VCCO_DDR_502_N6
R2	VCCO_DDR_502_R2
V1	VCCO_DDR_502_V1

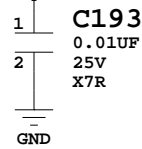
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SOC_IRON_CL484

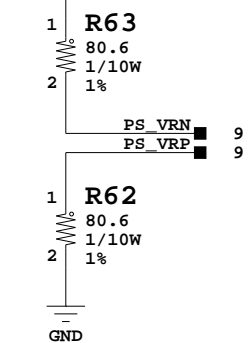
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VTTVREF_PS



VCC1V5_PS



Zynq Bank 502



Title: Zynq Bank 502 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM
 ASSY P/N: 0431696
 PCB P/N: 1280617
 SCH P/N: 0381449

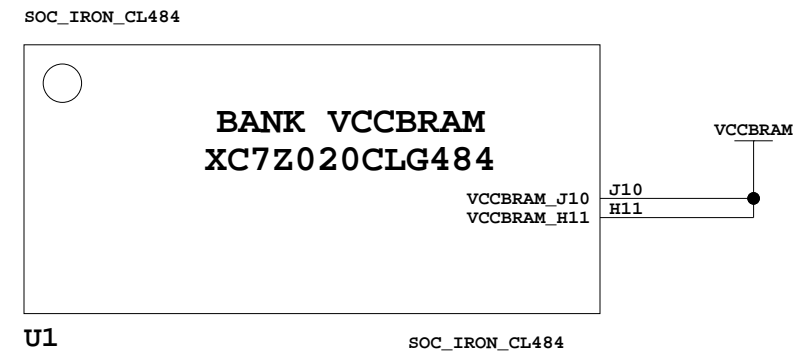
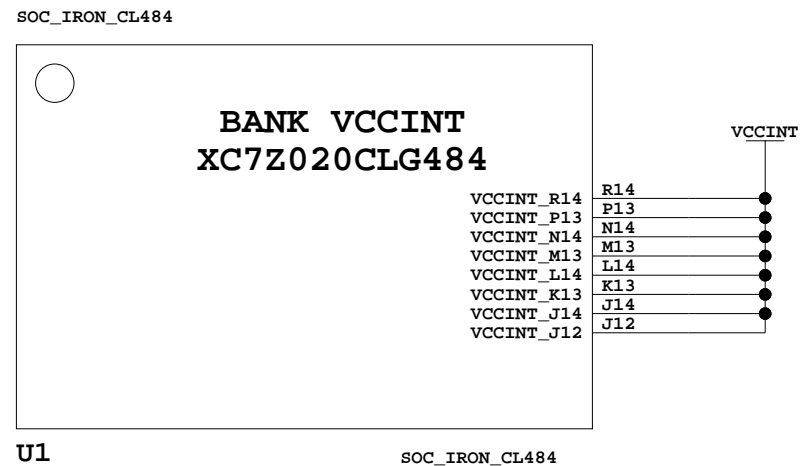
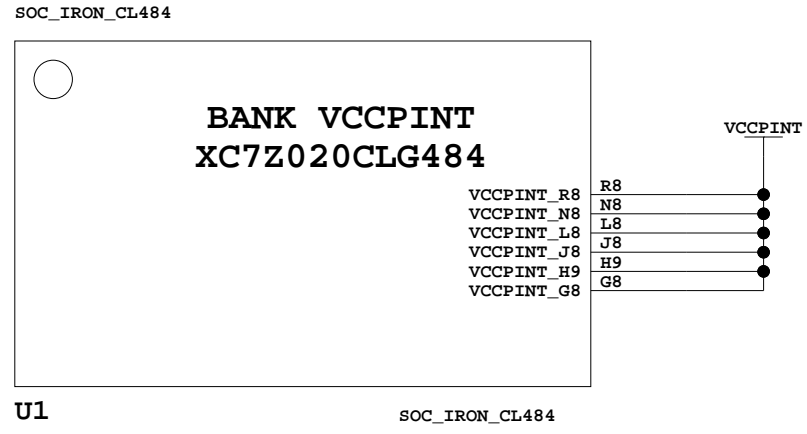
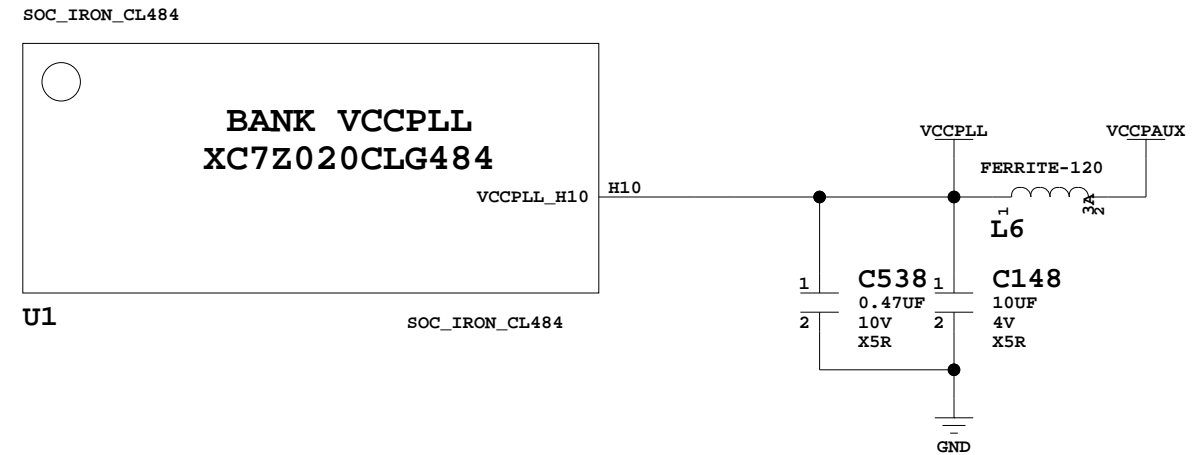
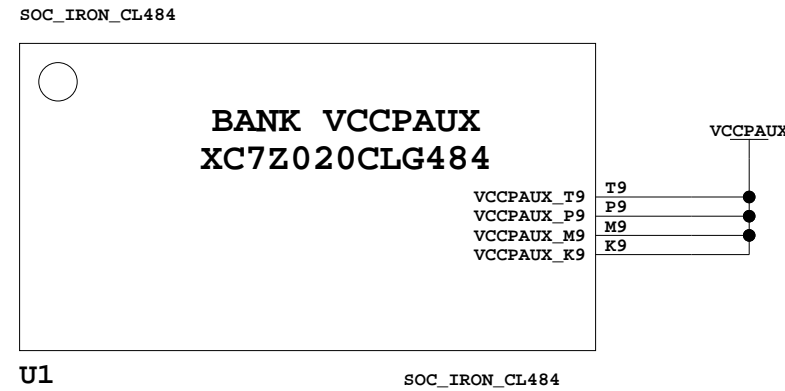
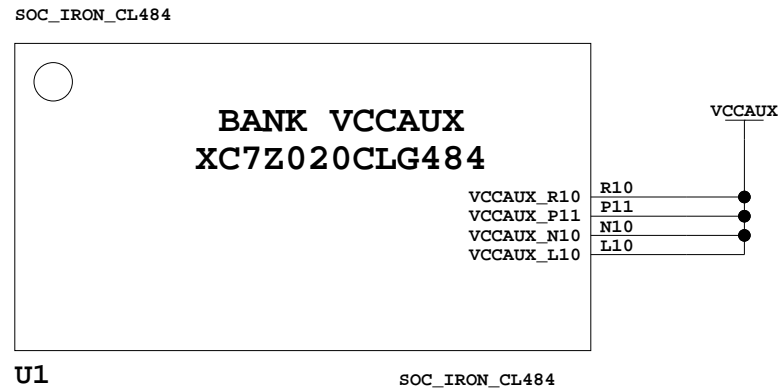
Date:	2-21-2013_17:10	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	9 of 48	Drawn By	BF

Increase width of VCCPLL route to as wide as possible (target is > 20 mils)

Reduce the length of VCCPLL route as much as possible

Place C538 inside the VIA field to provide as short as possible connection to VCCPLL (H10) and GND

Place C539 inside the open space cross adjacent to H10 for the short possible connection to VCCPLL

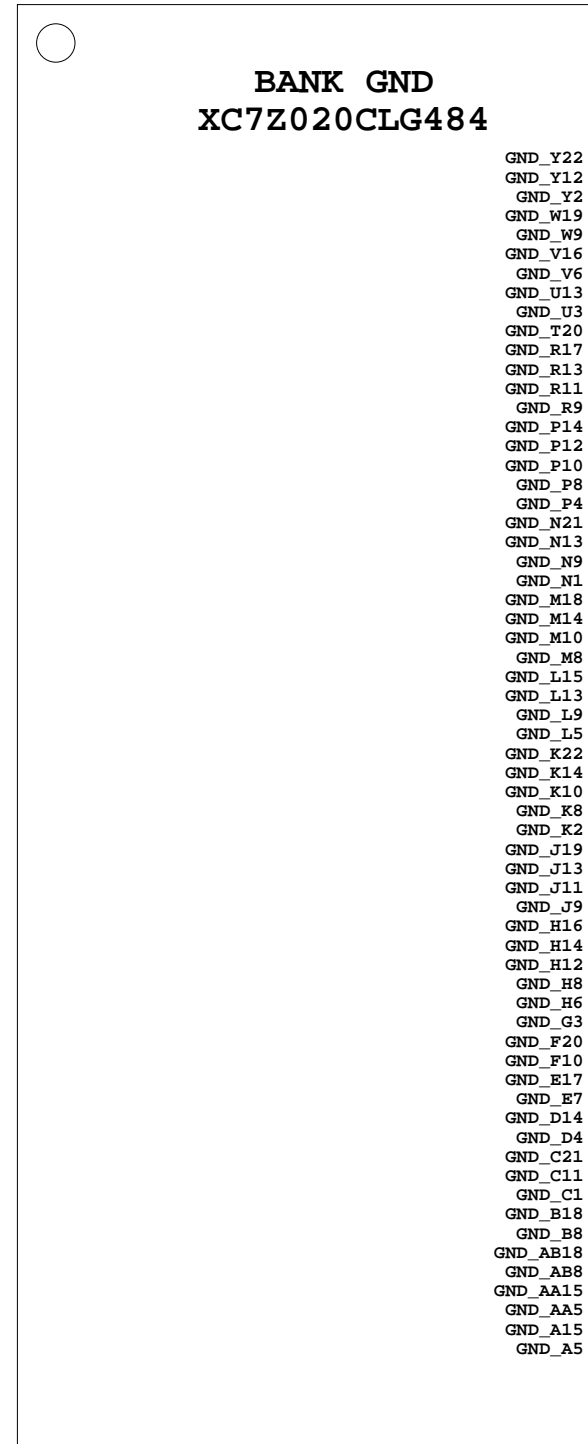


Zynq Power Pins



Title: Zynq Power Pins SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 10 of 48	Drawn By BF	

SOC_IRON_CL484



U1

SOC_IRON_CL484

GND

Zynq GND



Title:	Zynq GND SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
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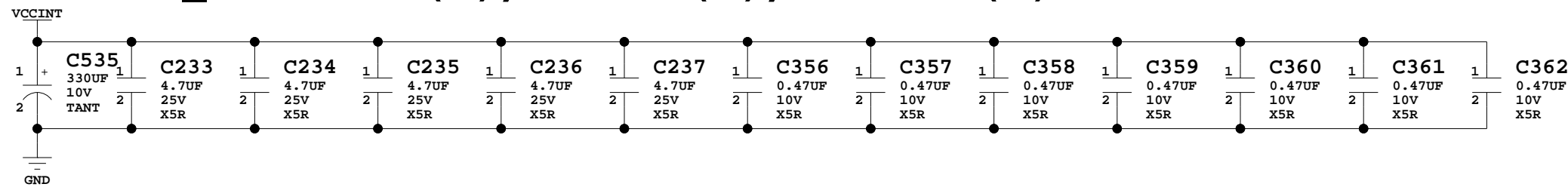
Date:	2-21-2013_17:10	Ver:	1.1
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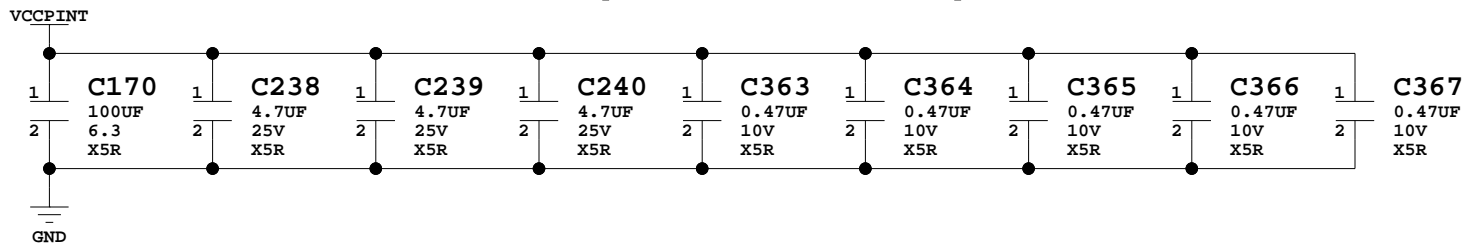
Sheet	11 of 48	Drawn By	BF
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BYPASS CAPACITORS

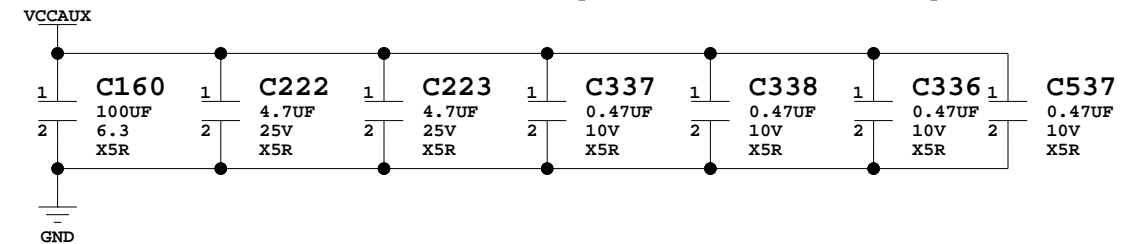
VCCINT_PL 330uF (1), 4.7uF (5), 0.47uF (7)



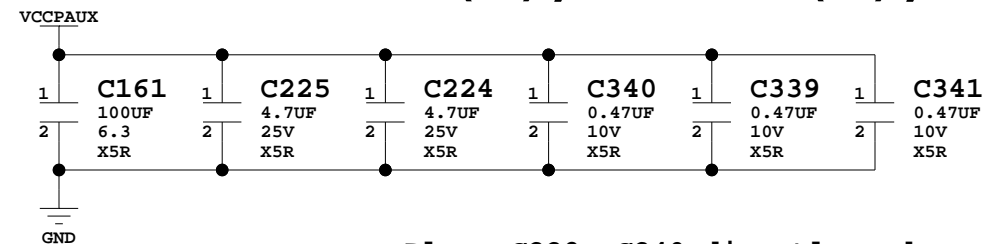
VCCPINT 100uF (1), 4.7uF (3), 0.47uF (5)



VCCAUX 100uF (1), 4.7uF (2), 0.47uF (4)

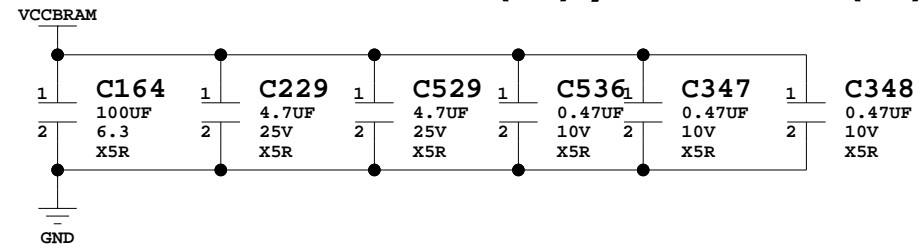


VCCPAUX 100uF (1), 4.7uF (2), 0.47uF (3)

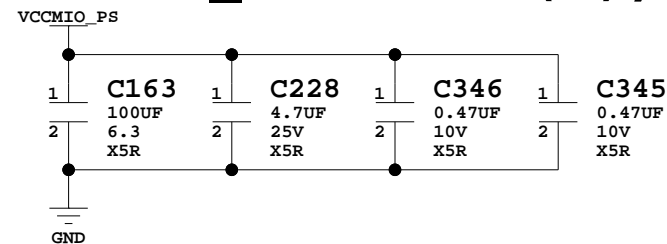


Place C339, C340 directly underneath the FPGA as short as possible connection to VCCPAUX and GND

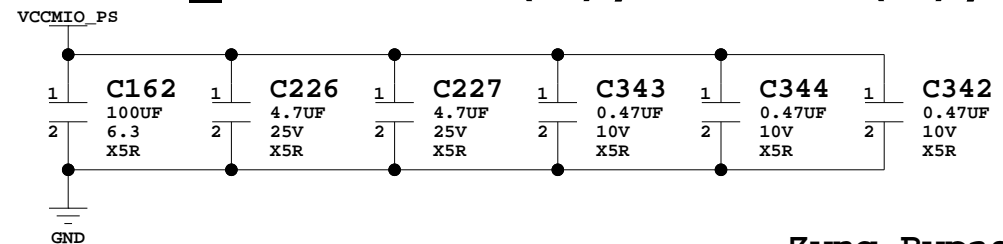
VCCBRAM 100uF (1), 4.7uF (2), 0.47uF (3)



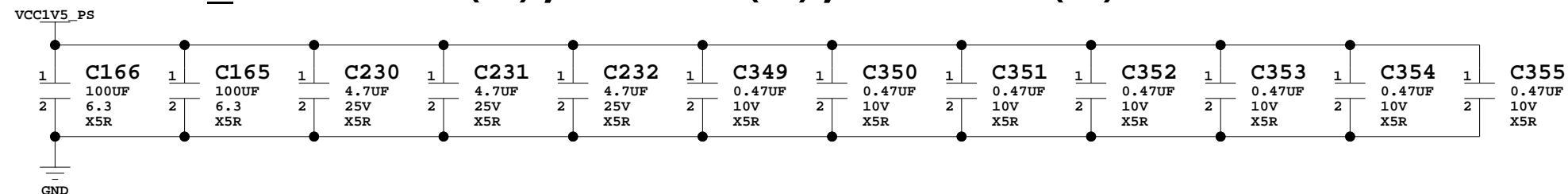
VCCP0_PS 100uF (1), 4.7uF (1), 0.47uF (2)



VCCP1_PS 100uF (1), 4.7uF (2), 0.47uF (3)



VCC1V5_PS 100uF (2), 4.7uF (3), 0.47uF (7)



Zynq Bypass Capacitors

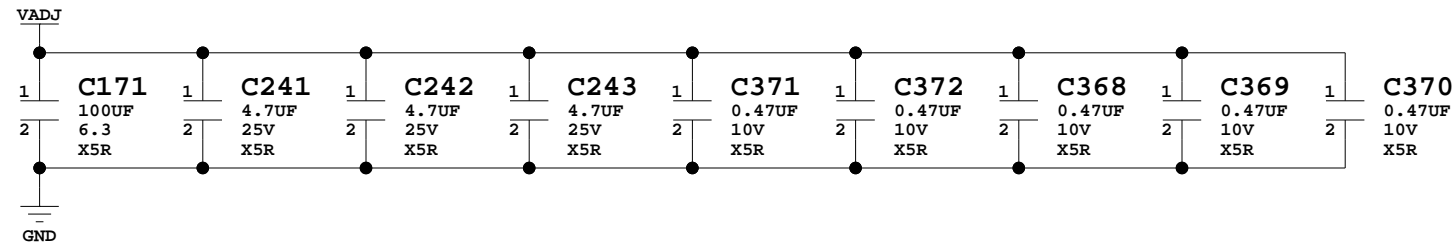


Title: Zynq Bypass Capacitors
SCHEM, ROHS COMPLIANT
ZC702 EVALUATION PLATFORM

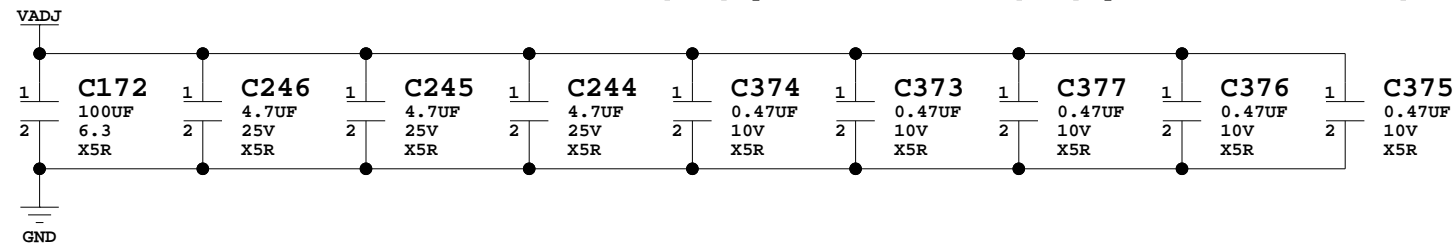
ASSY P/N: 0431696
PCB P/N: 1280617
SCH P/N: 0381449

Date:	2-21-2013_17:10	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	12 of 48	Drawn By	BF

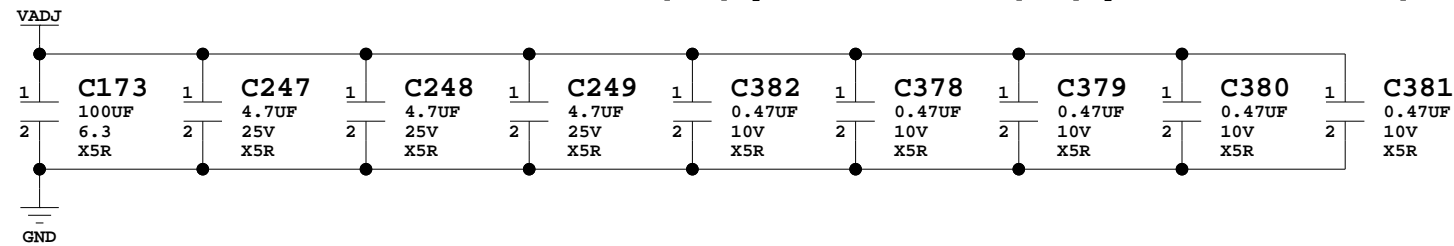
Bank 13 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



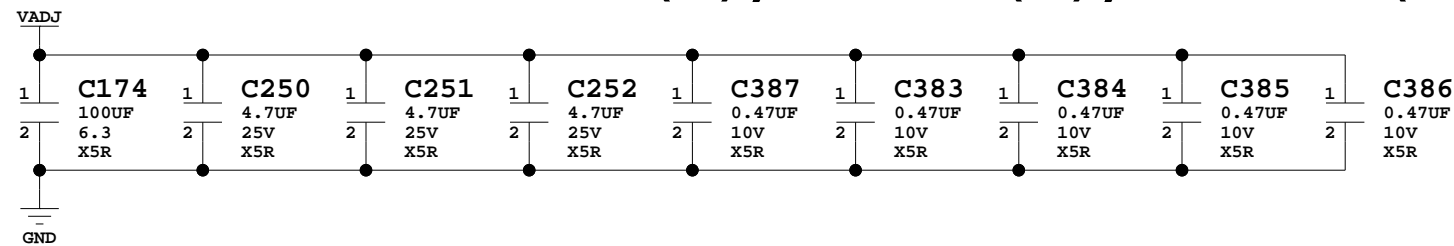
Bank 33 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



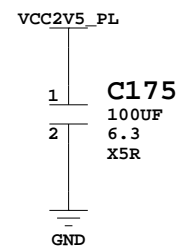
Bank 34 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



Bank 35 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



VCC2V5_PL 100uF (1)

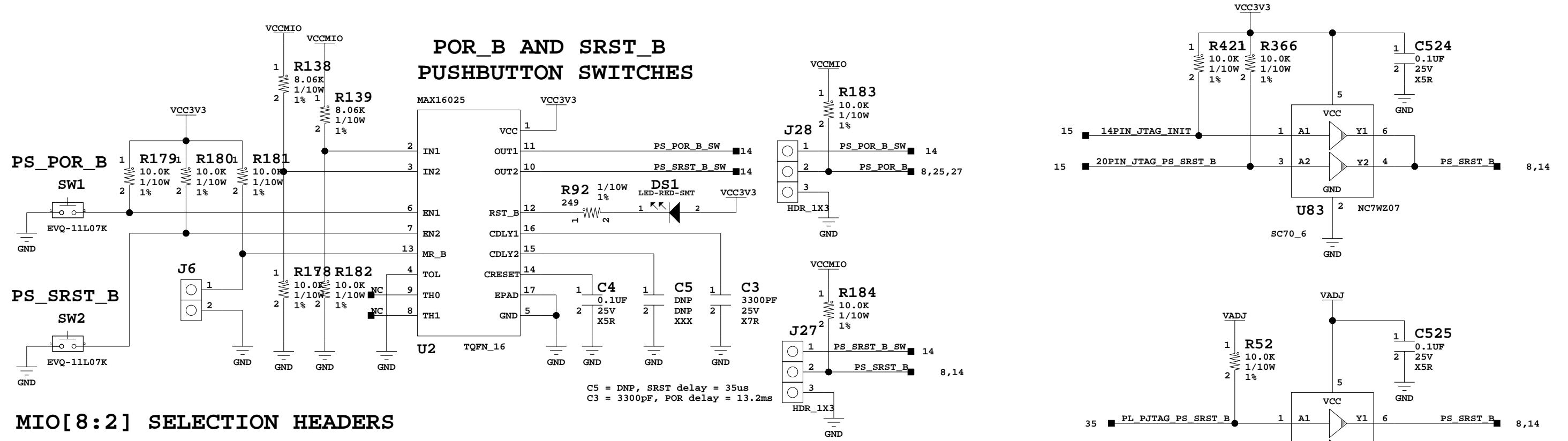


Zynq Bypass Capacitors

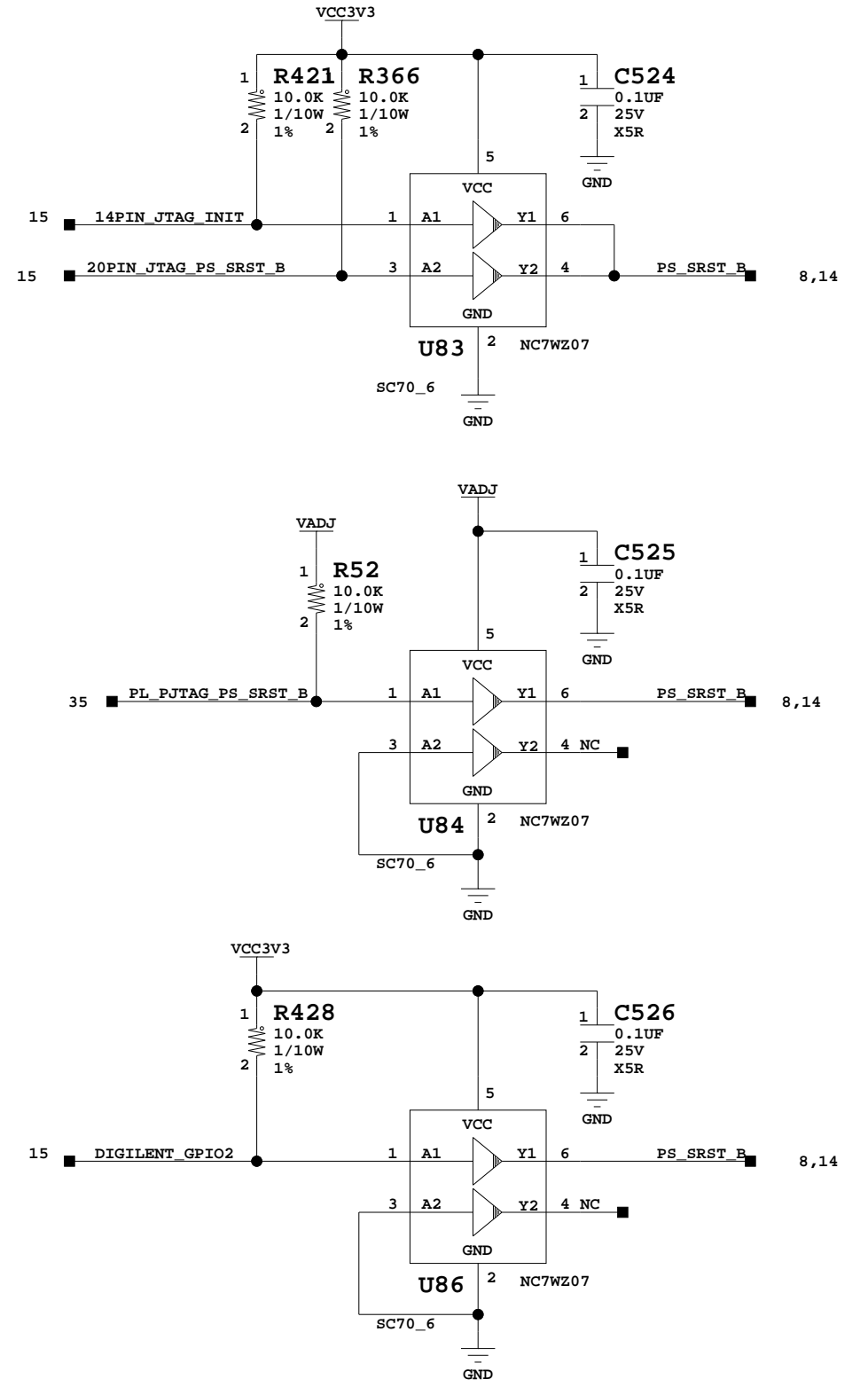
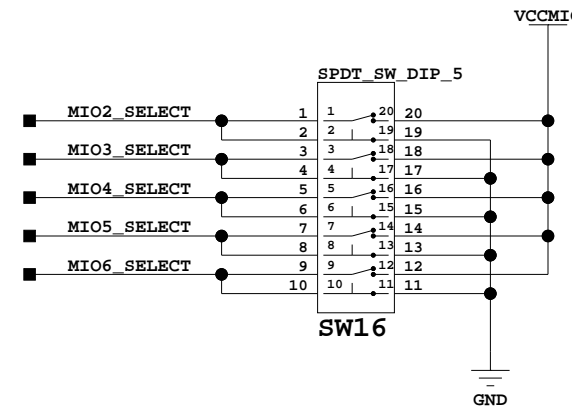
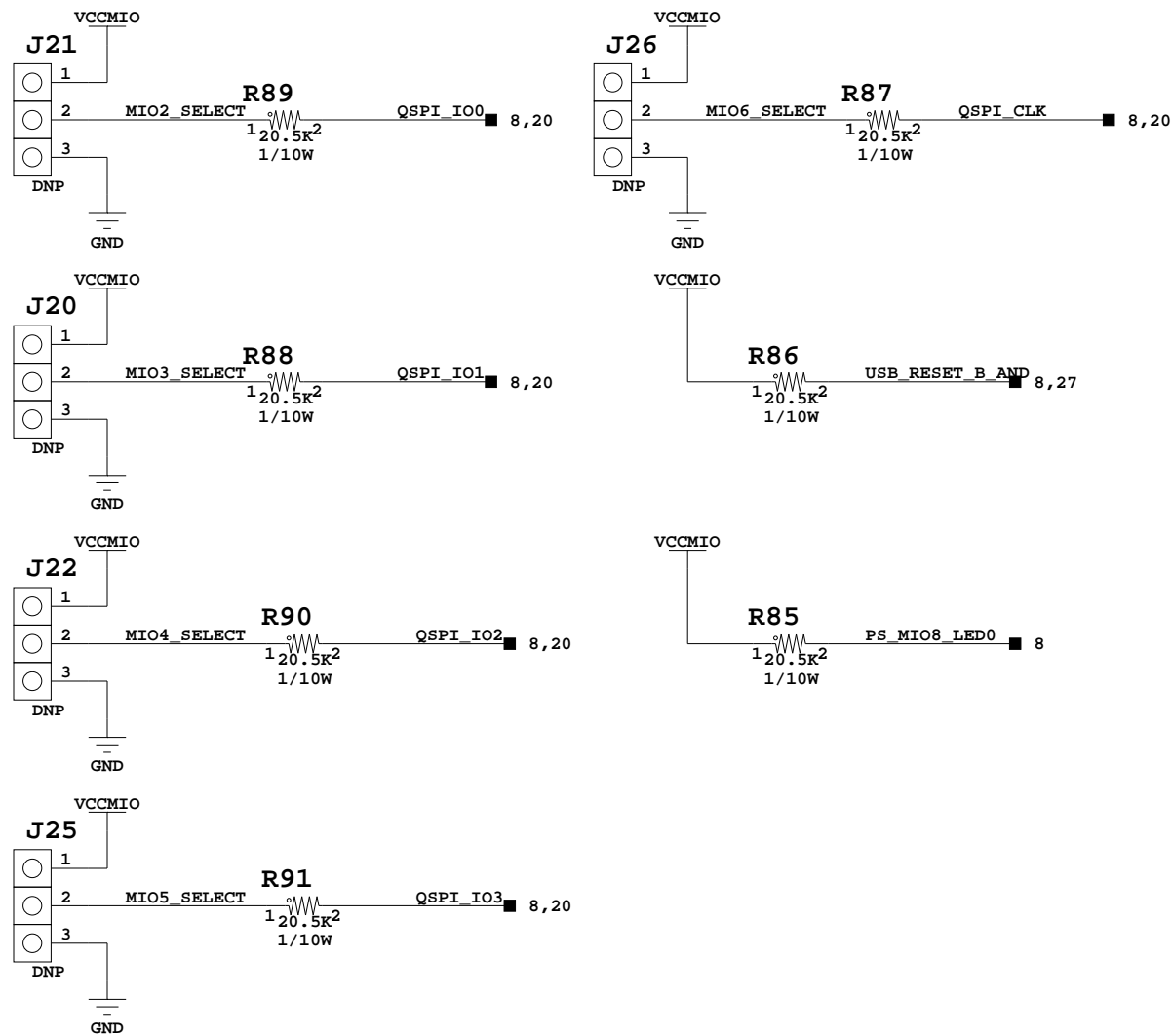


Title: Zynq Bypass Capacitors SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 13 of 48	Drawn By BF	

POR_B AND SRST_B PUSHBUTTON SWITCHES



MIO[8:2] SELECTION HEADERS

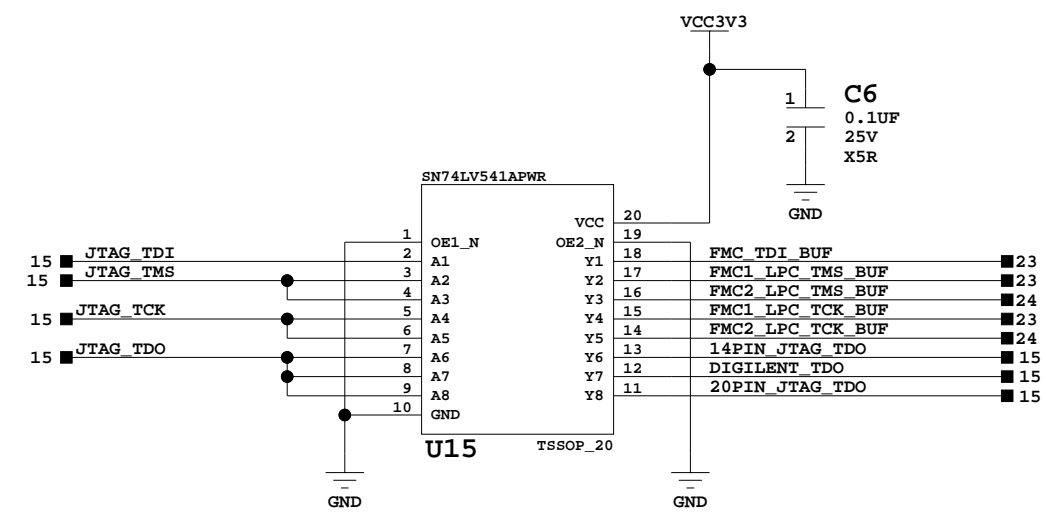
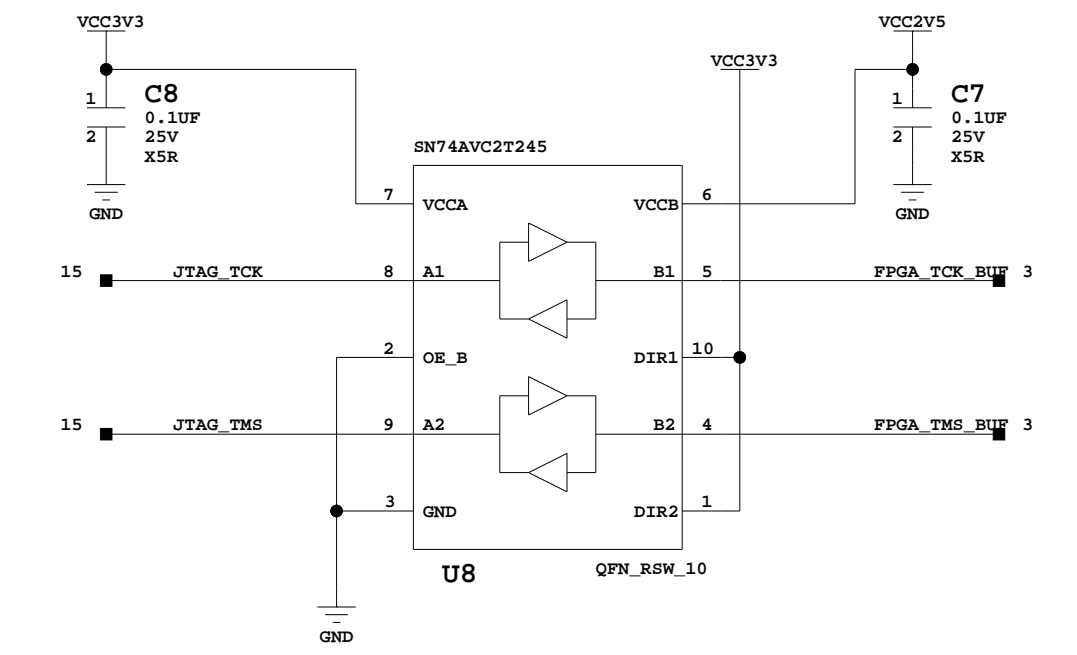
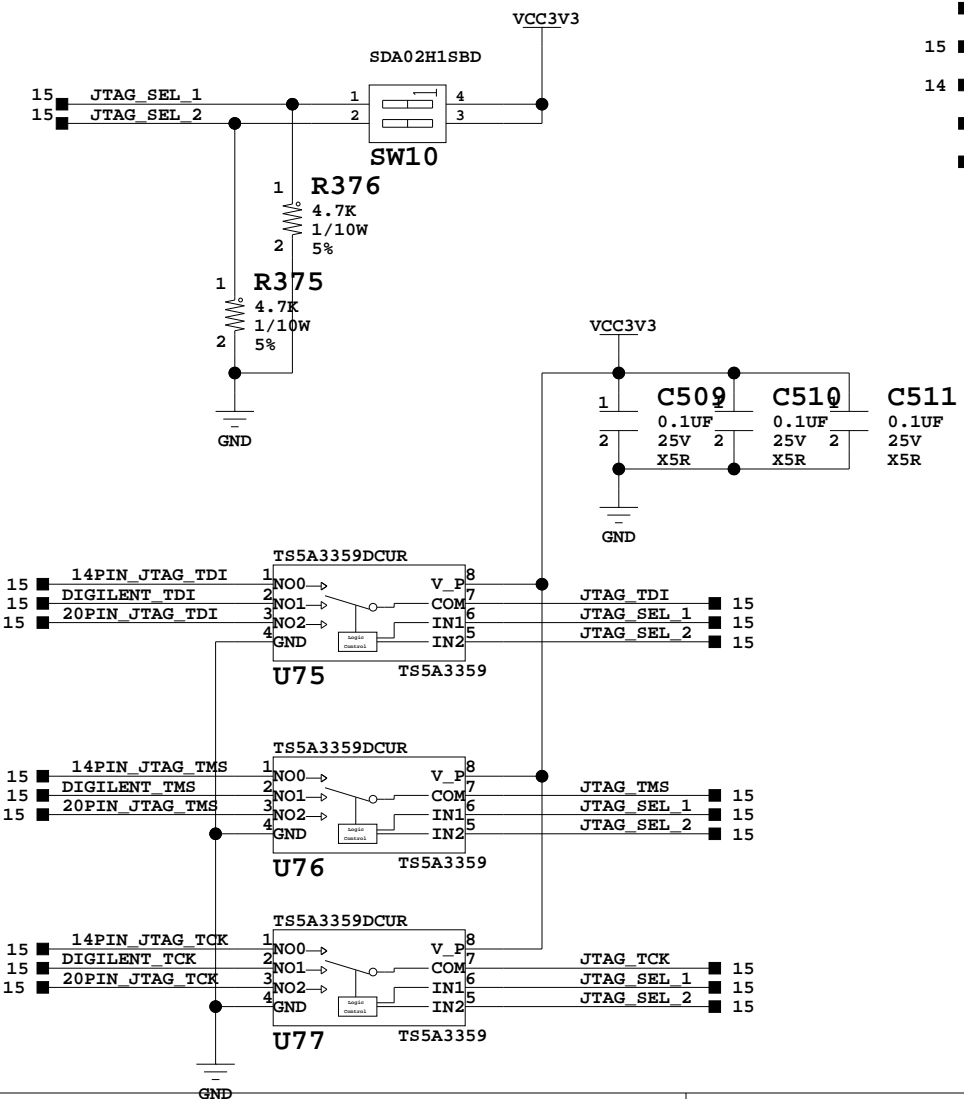
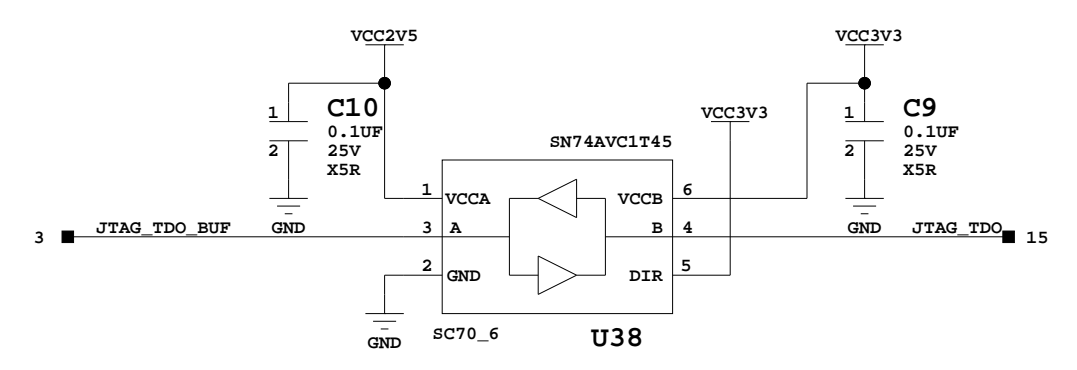
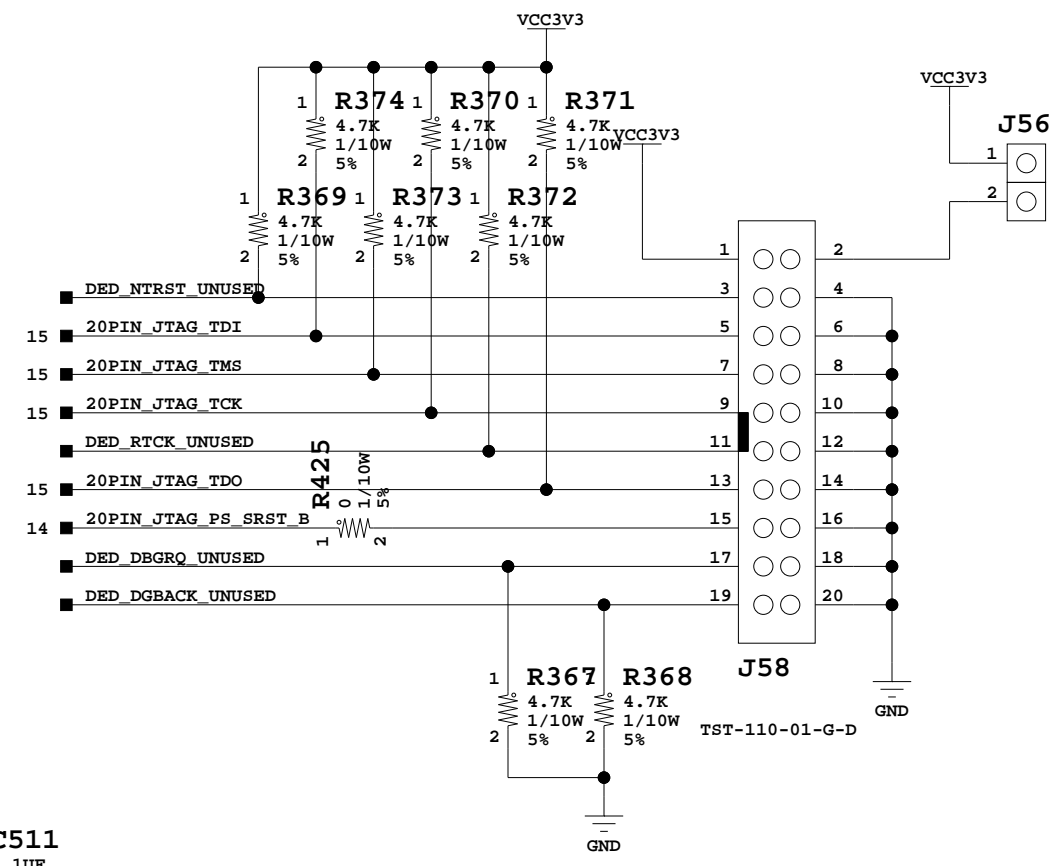
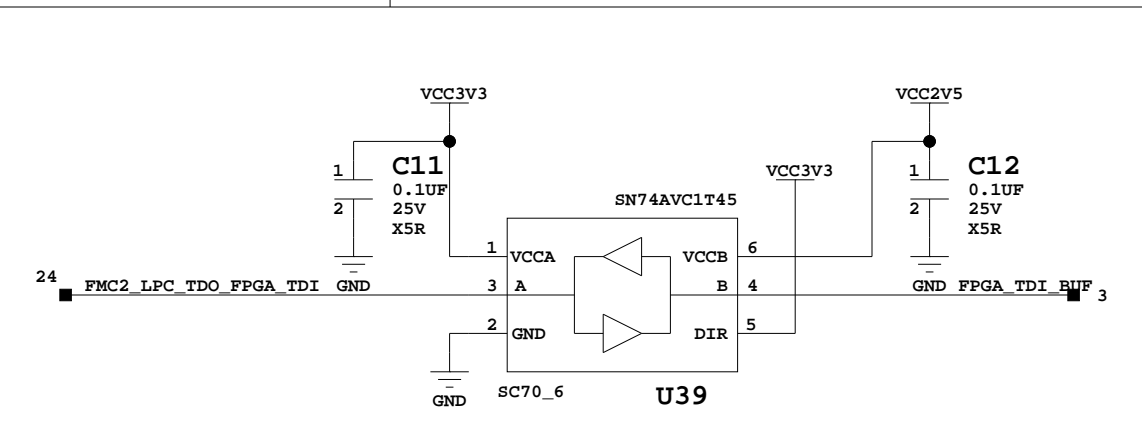
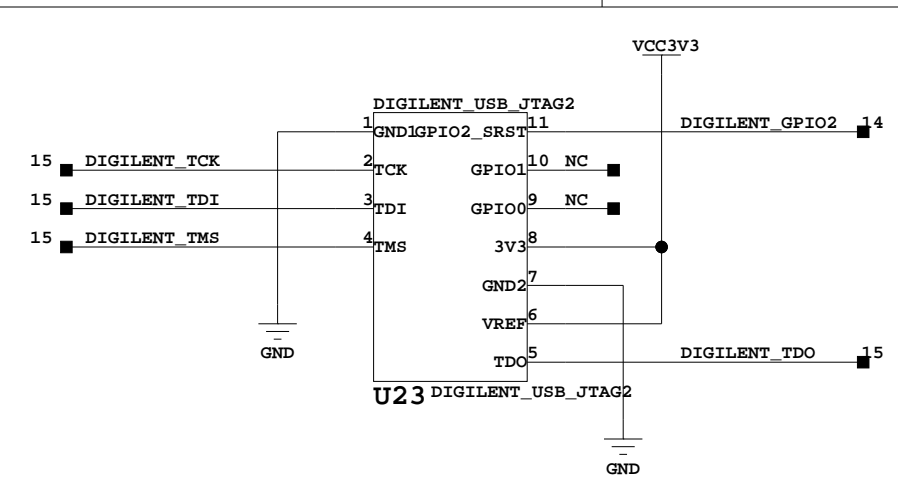
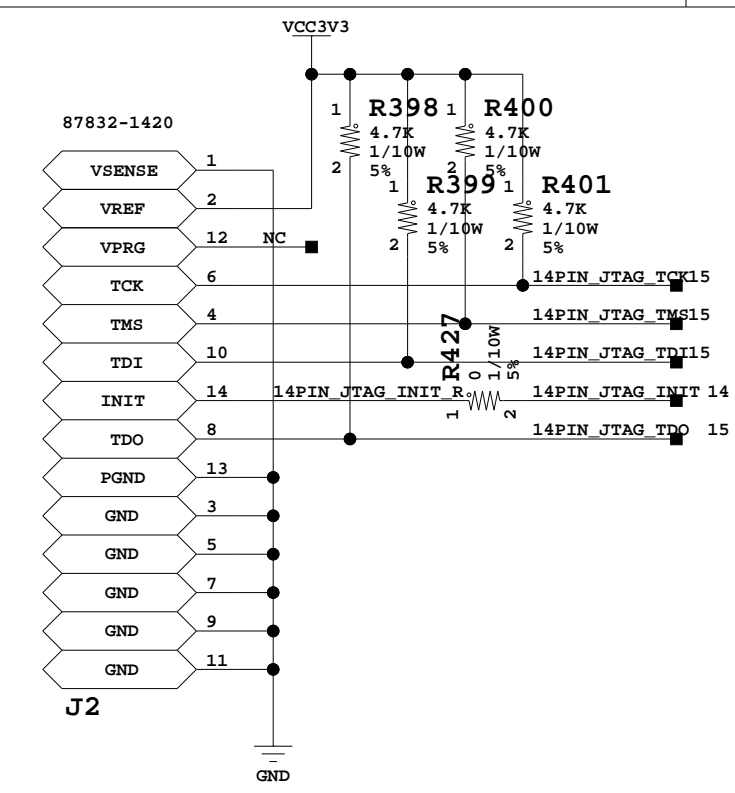


Power Supervisor, Zynq Config Pins, ResetASSY



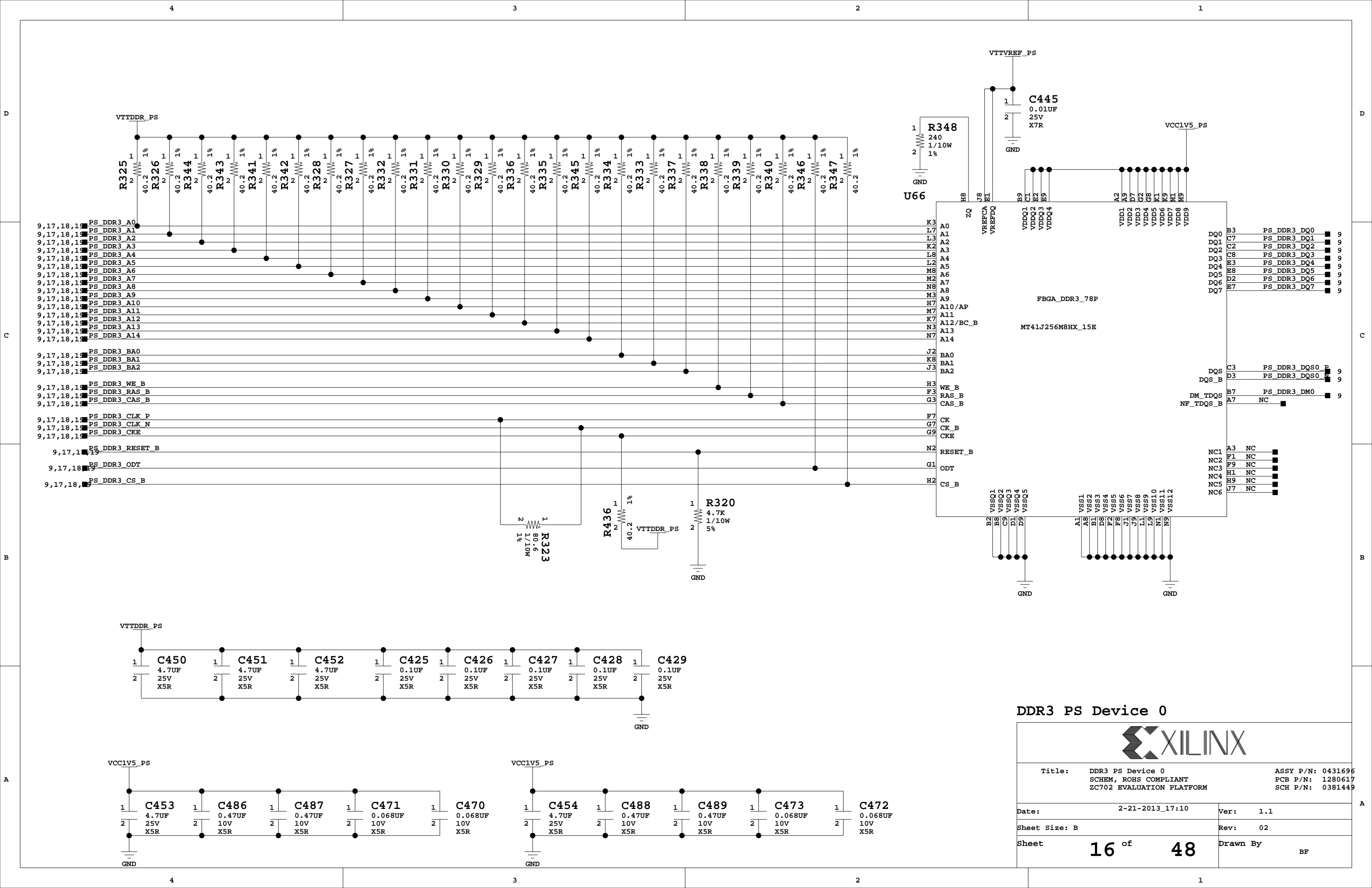
Title: Power Supervisor, Zynq Config Pins, ResetASSY P/N: 0431696
SCHEM, ROHS COMPLIANT PCB P/N: 1280617
ZC702 EVALUATION PLATFORM SCH P/N: 0381449

Date:	2-21-2013_17:10	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	14 of 48	Drawn By	BF



JTAG Buffer, USB JTAG Module, JTAG Hdr

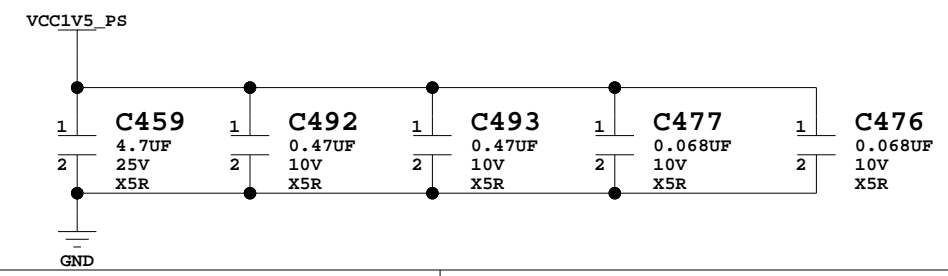
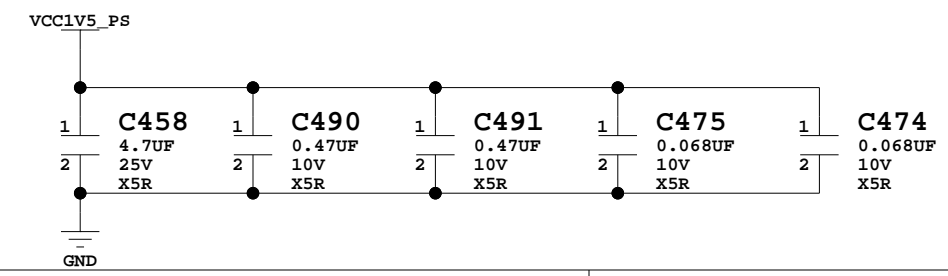
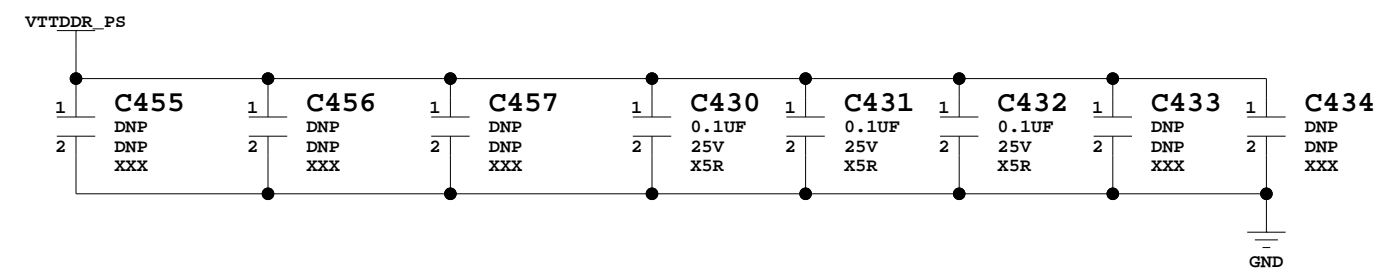
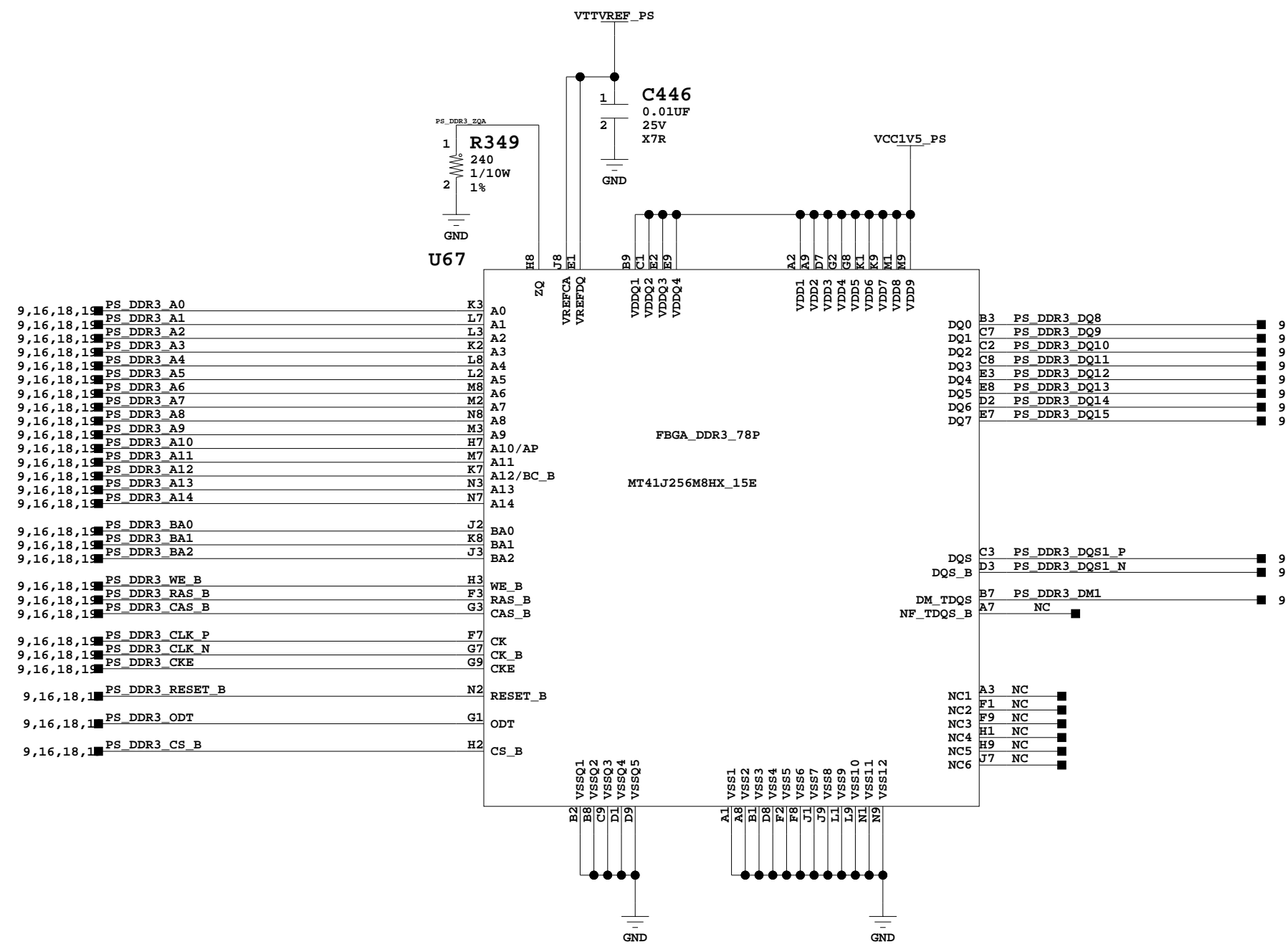
Title: JTAG Buffer, USB JTAG Module, JTAG Hdr ASSY P/N: 0431696 SCHEM, ROHS COMPLIANT PCB P/N: 1280617 ZC702 EVALUATION PLATFORM SCH P/N: 0381449	
Date: 2-21-2013_17:10	Ver: 1.1
Sheet Size: B	Rev: 02
Sheet 15 of 48	Drawn By BF



DDR3 PS Device 0



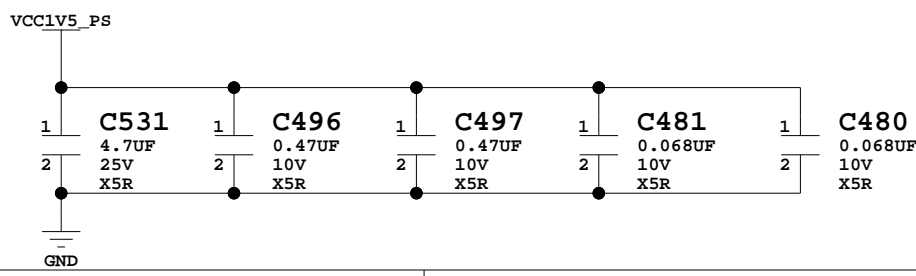
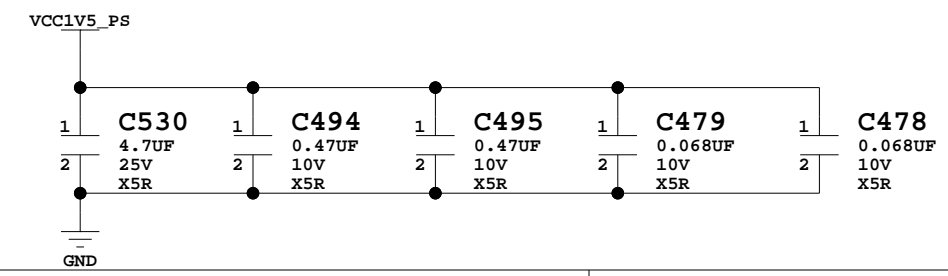
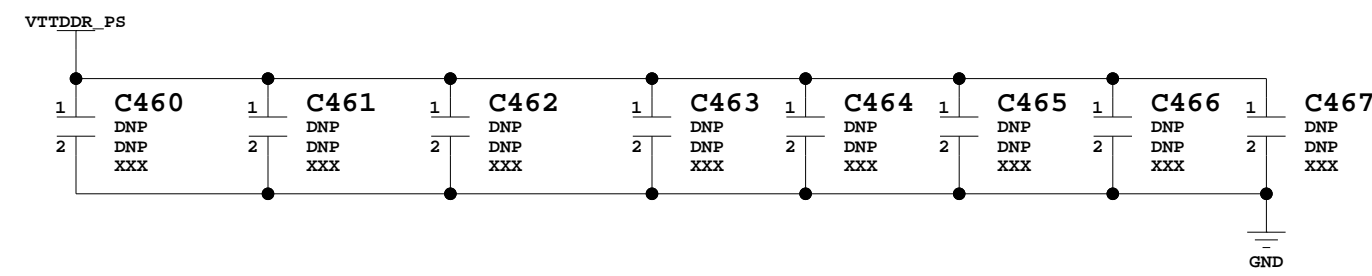
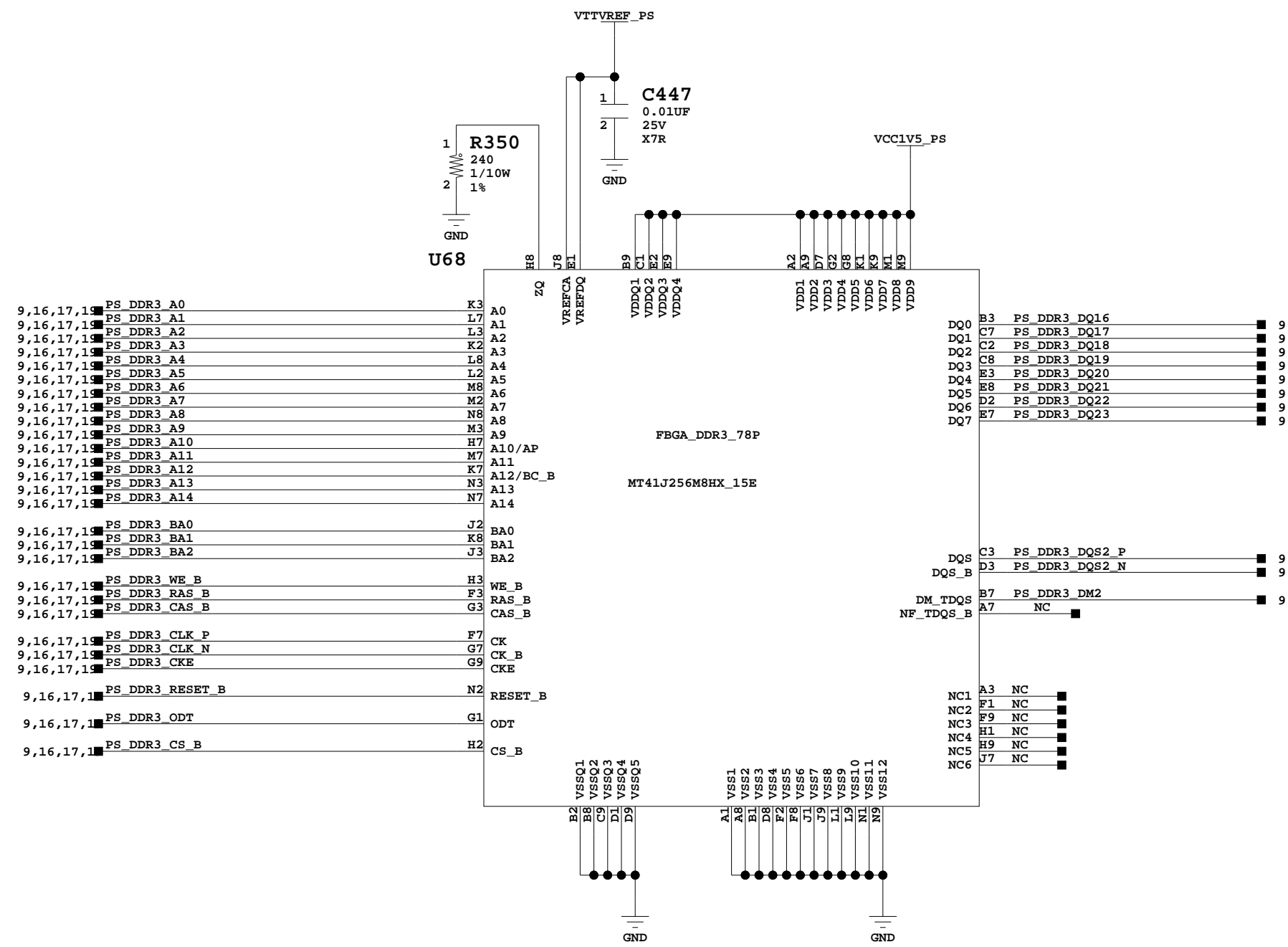
Title: DDR3 PS Device 0		ASSY P/N: 0431696
SCHEM, ROHS COMPLIANT		PCB P/N: 1280617
ZC702 EVALUATION PLATFORM		SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 16 of 48	Drawn By BF	



DDR3 PS Device 1



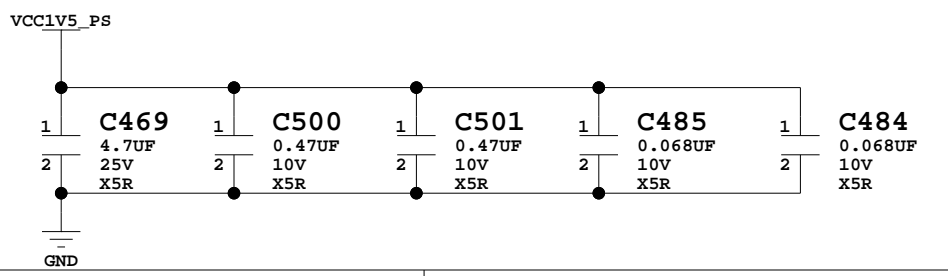
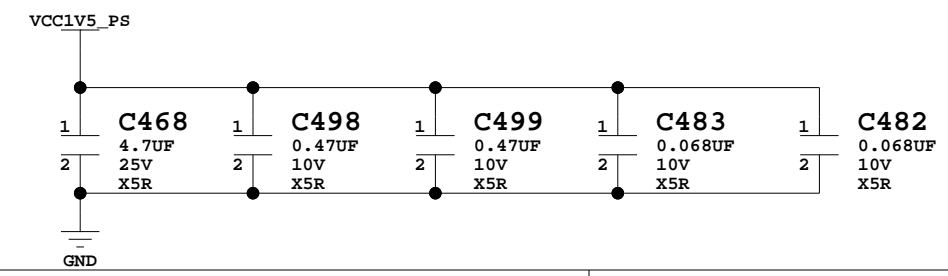
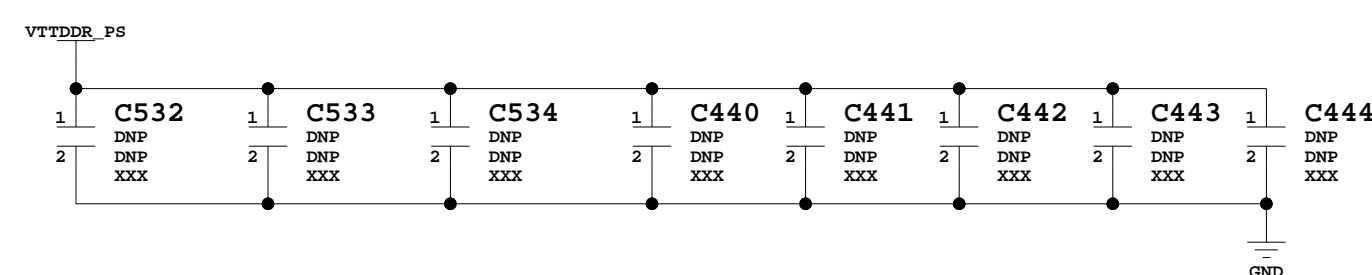
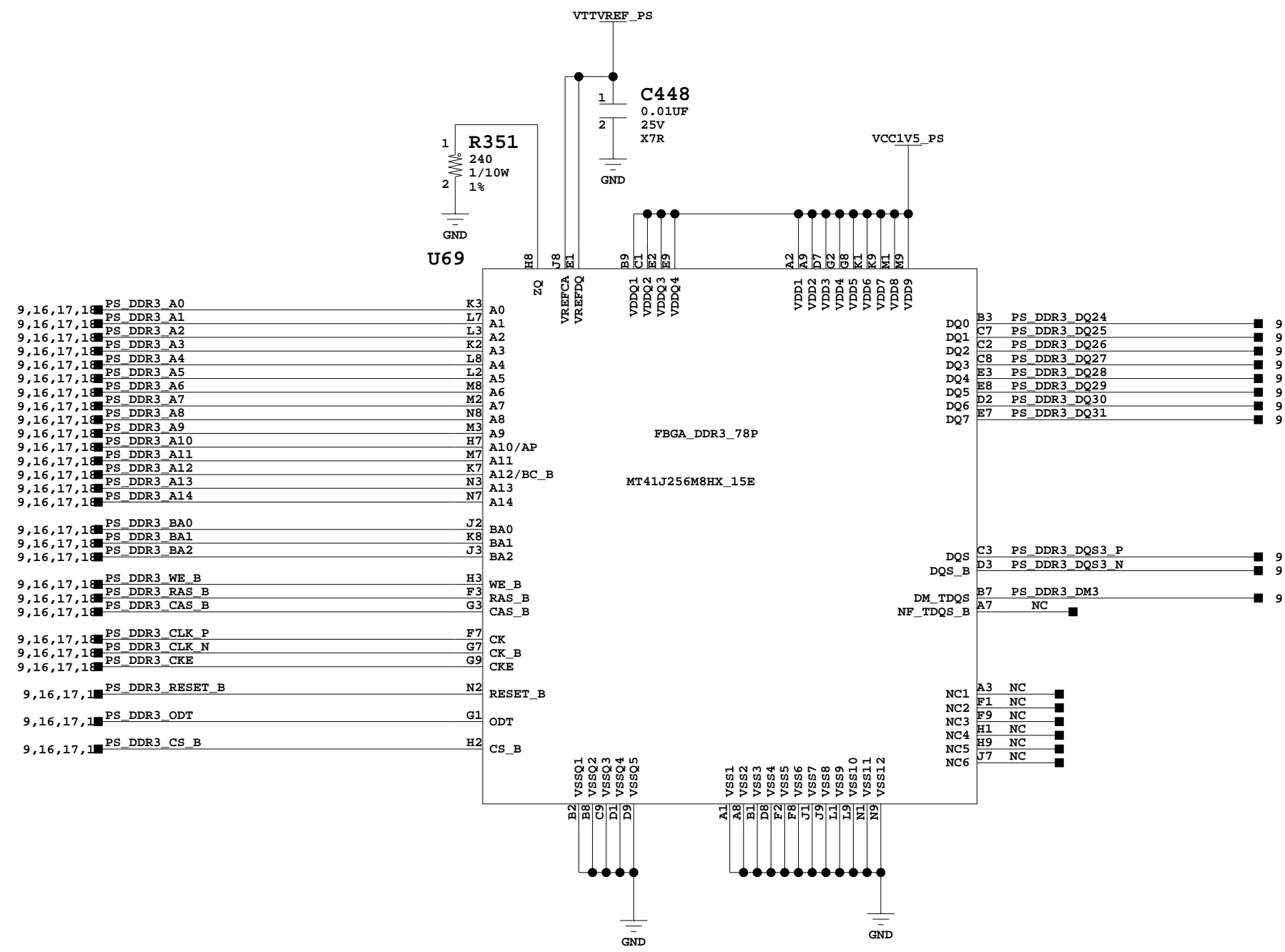
Title: DDR3 PS Device 1 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 17 of 48	Drawn By BF	



DDR3 PS Device 2



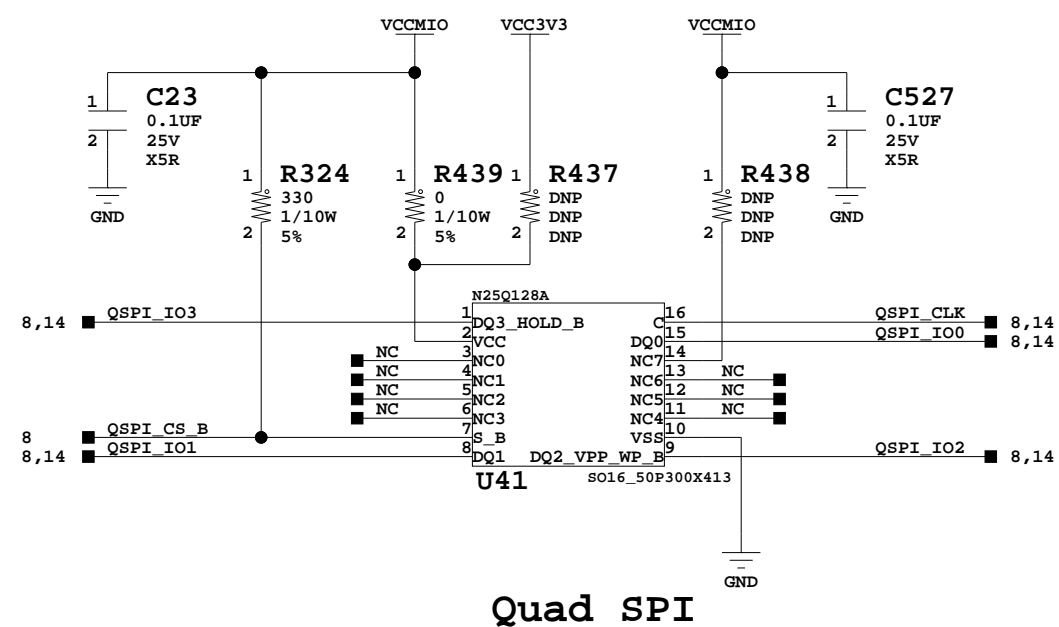
Title: DDR3 PS Device 2 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 18 of 48	Drawn By BF	



DDR3 PS Device 3



Title: DDR3 PS Device 3 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 19 of 48	Drawn By BF	

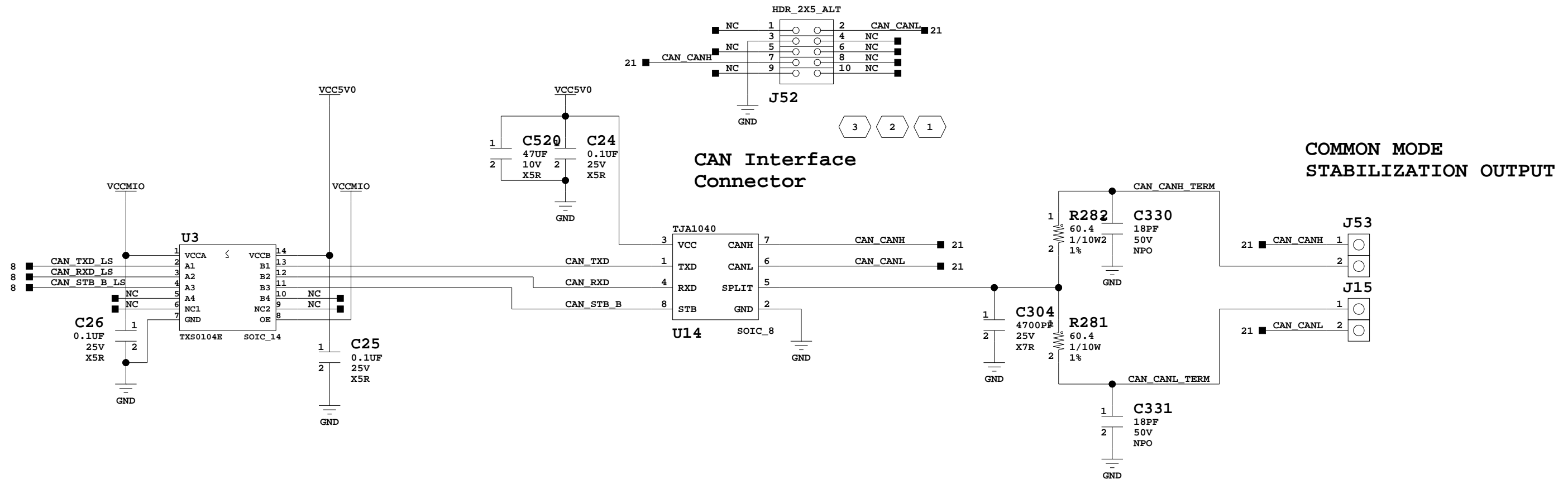


Quad SPI

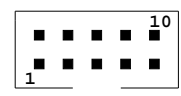
Quad SPI



Title: Quad SPI SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 20 of 48	Drawn By BF	



3 THE CONNECTOR PIN ORDER WITH RESPECT TO THE KEYWAY IS SHOWN HERE:



CONNECTOR (TOP VIEW)

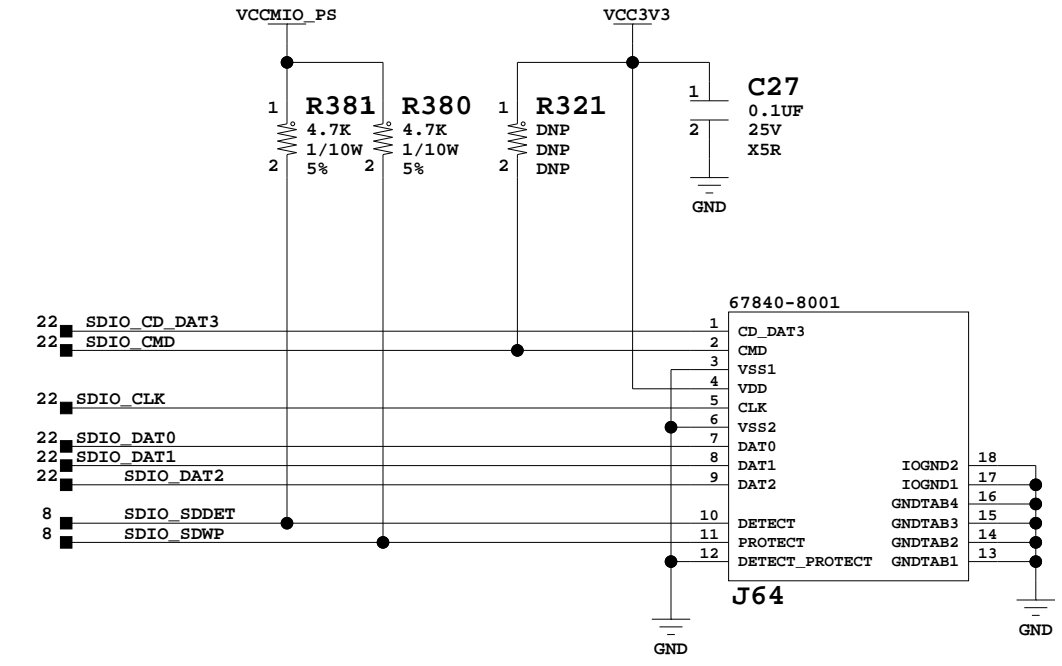
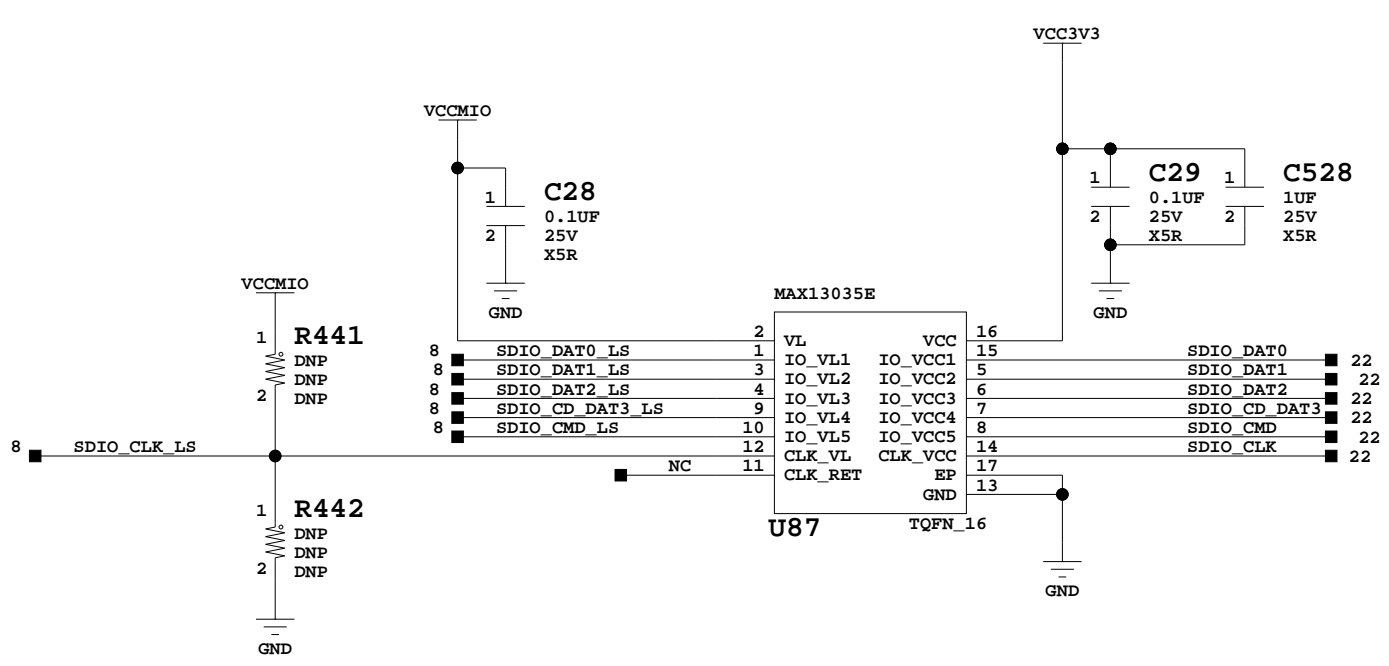
2 CONNECTOR IS INTENDED TO MATE WITH PCCABLES.COM CABLE P/N 07120.

1 CO-LOCATE CAN INTERFACE CONNECTOR AND C/M STABILIZATION OUTPUT 2X1 HEADER

CAN Bus



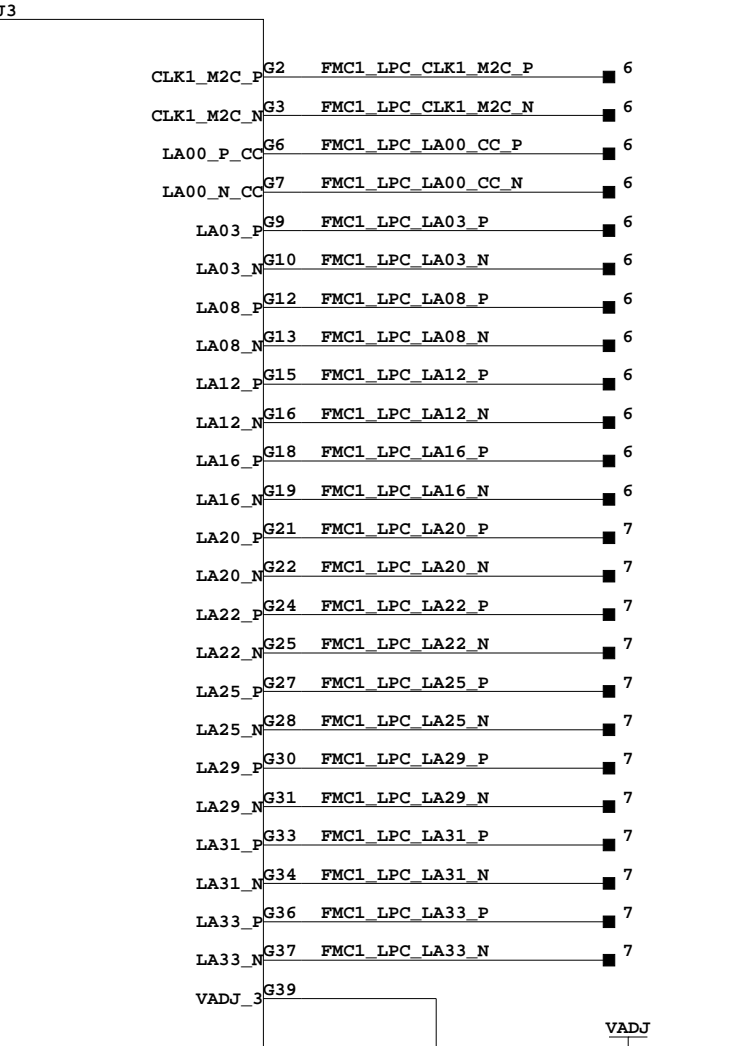
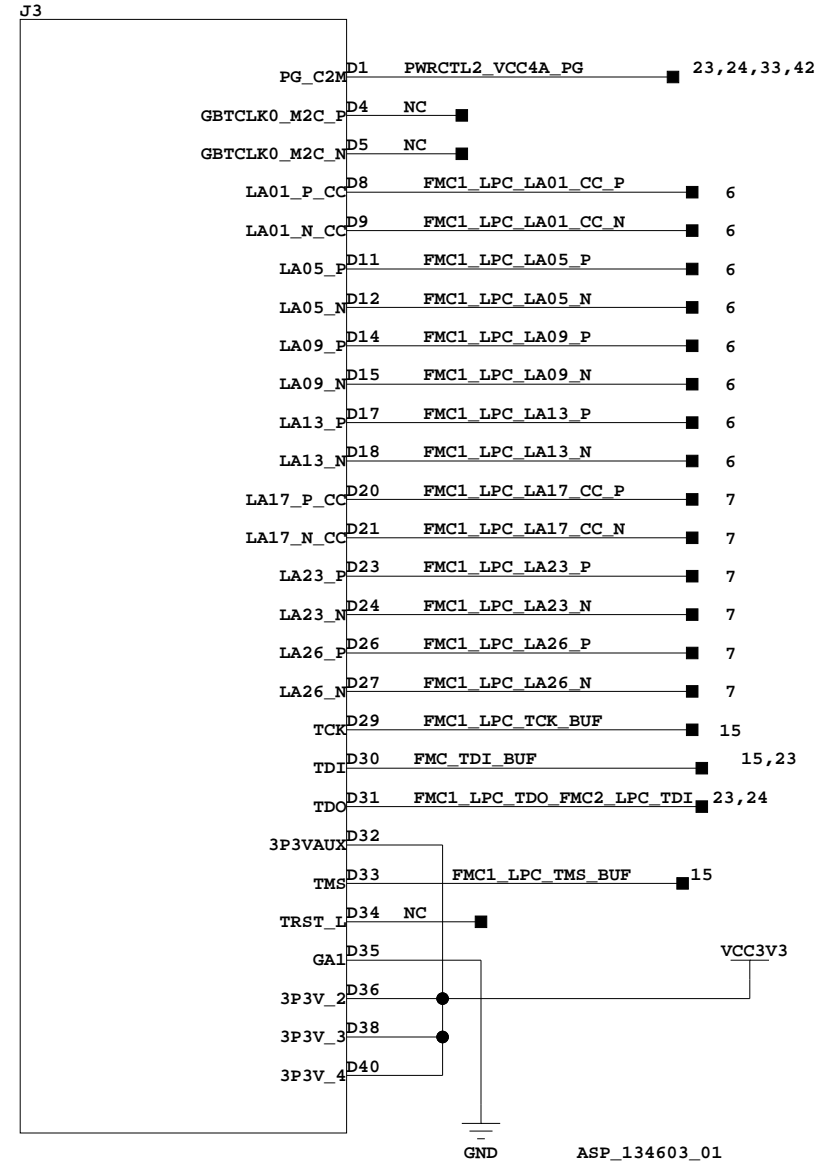
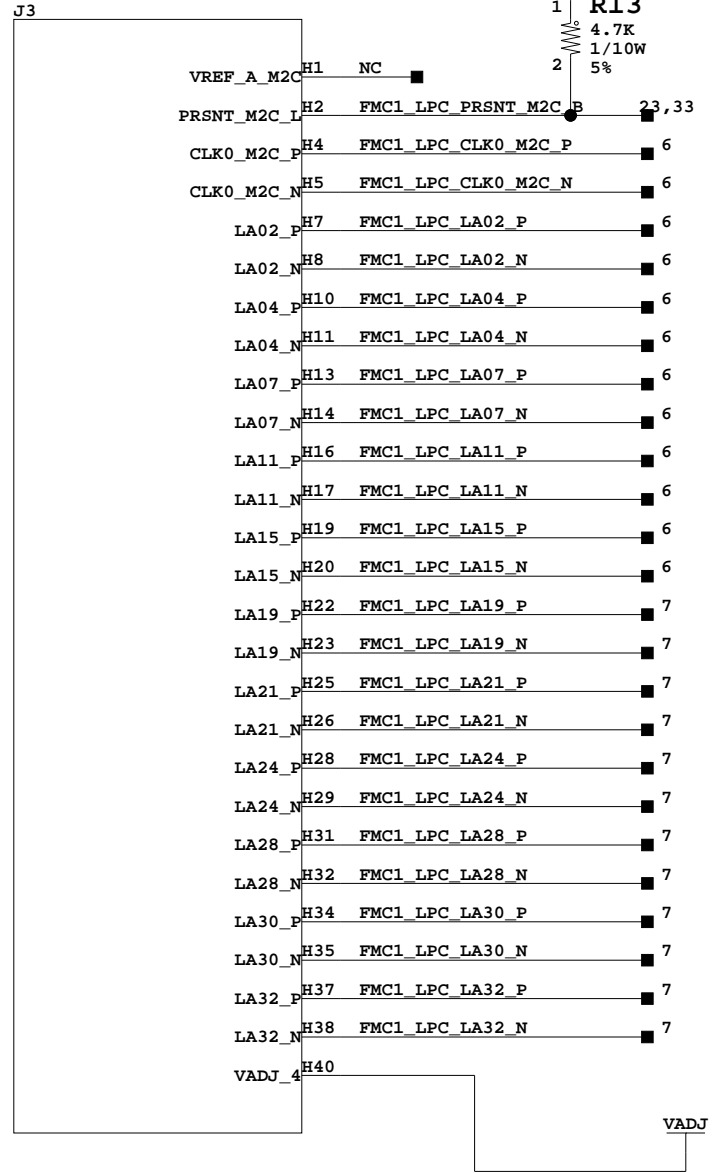
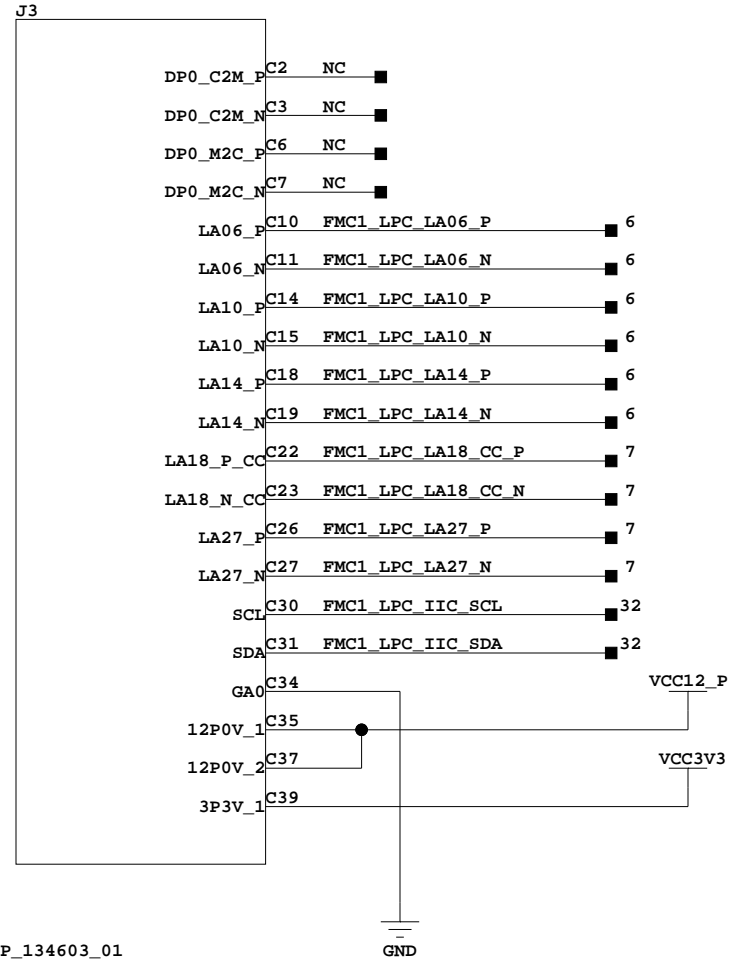
Title: CAN Bus SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 21 of 48	Drawn By BF	



SD Card Connector



Title: SD Card Connector SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 22 of 48	Drawn By BF	

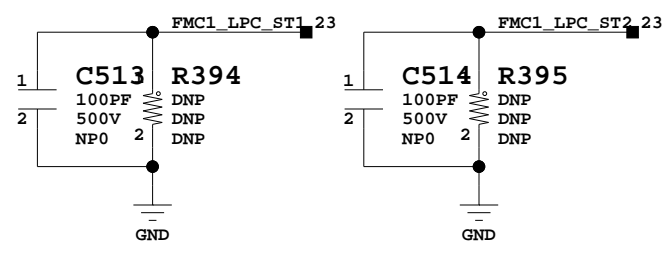


ASP_134603_01

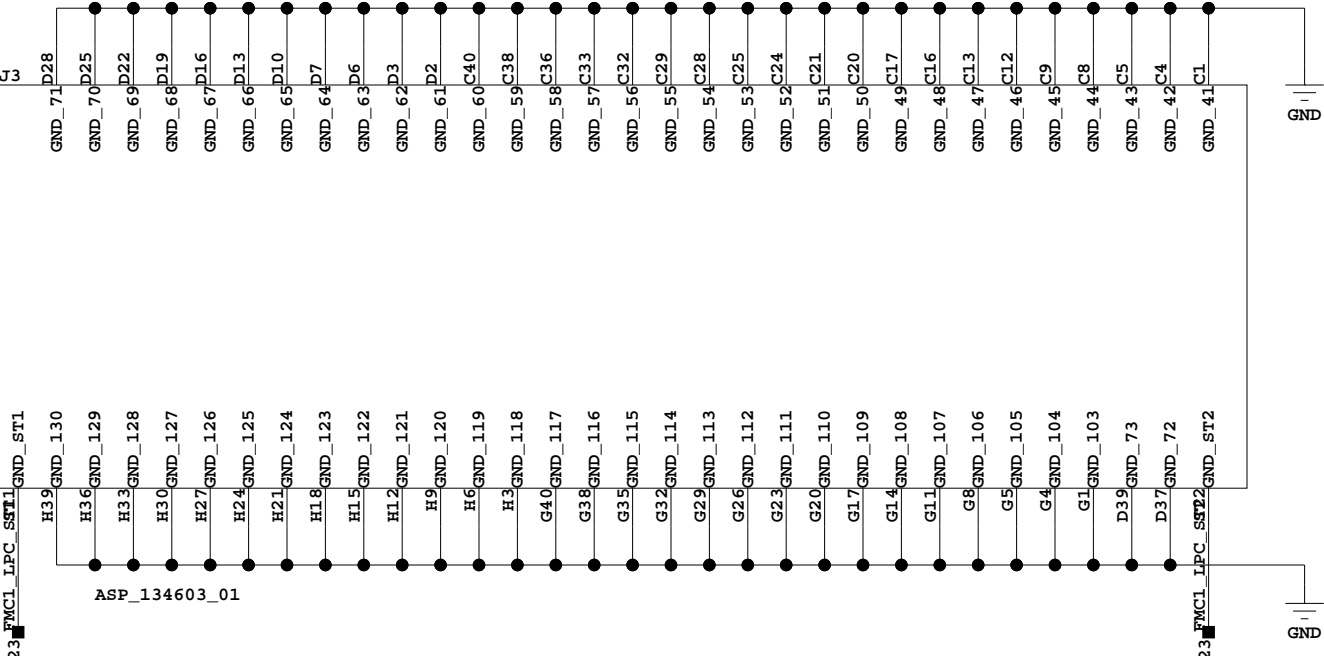
ASP_134603_01

ASP_134603_01

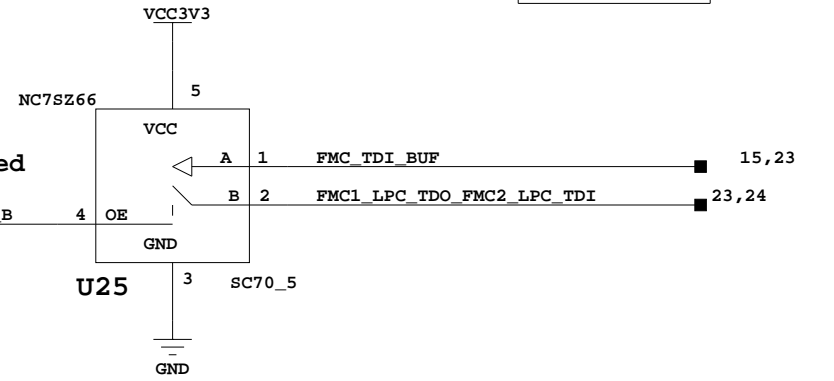
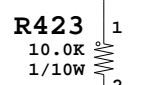
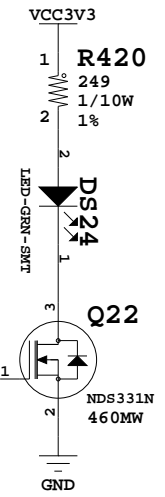
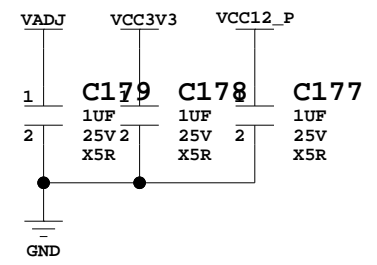
ASP_134603_01



ASP_134603_01



ASP_134603_01

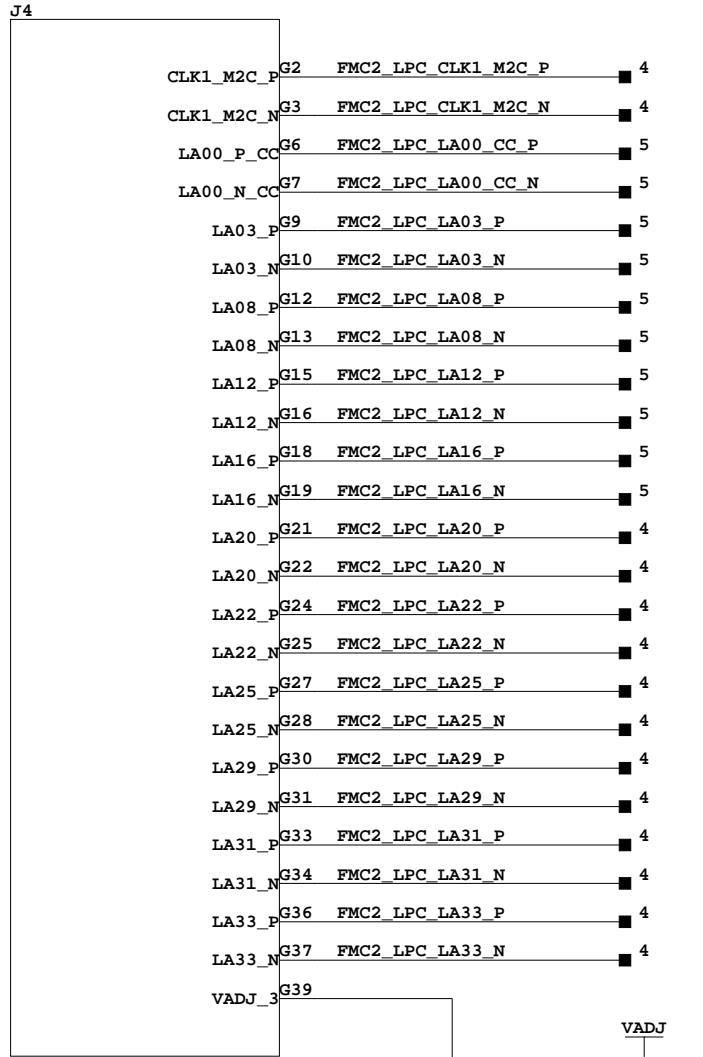
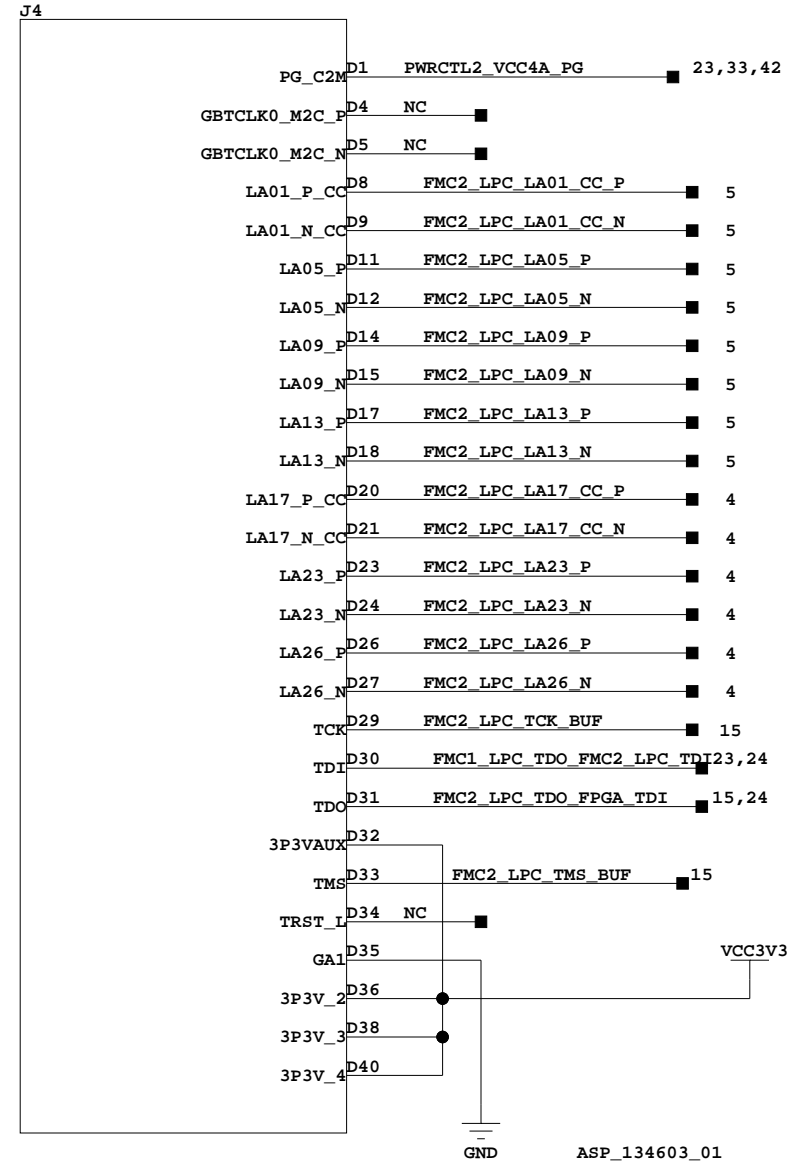
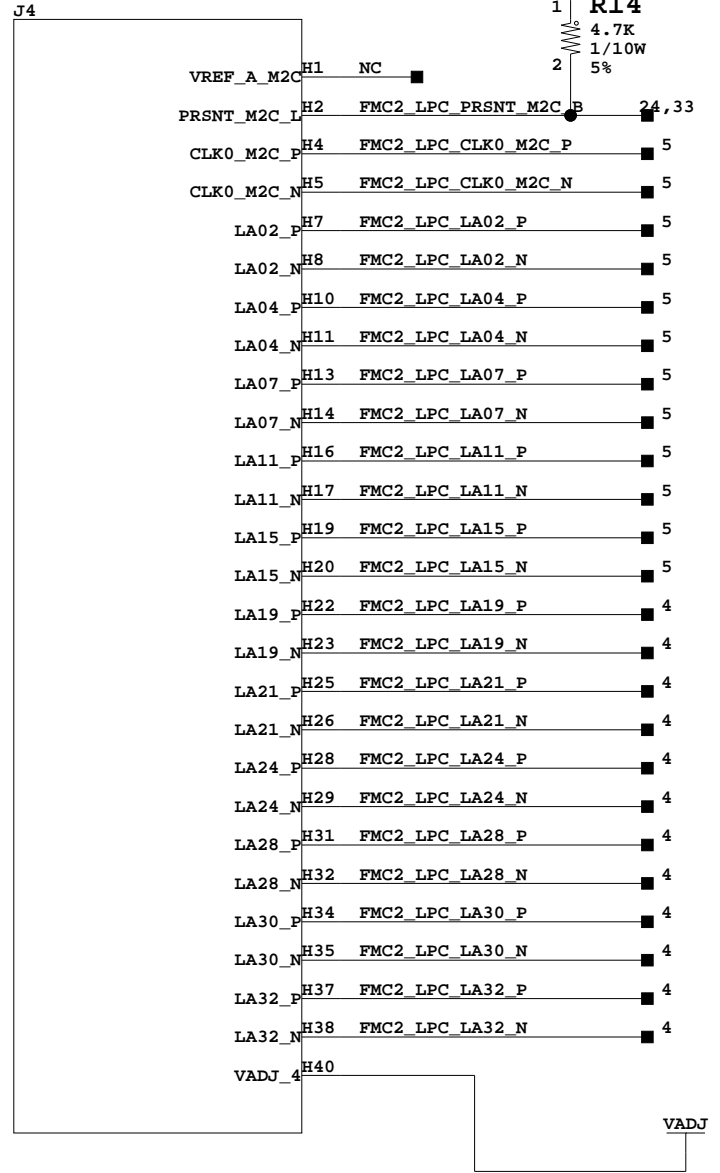
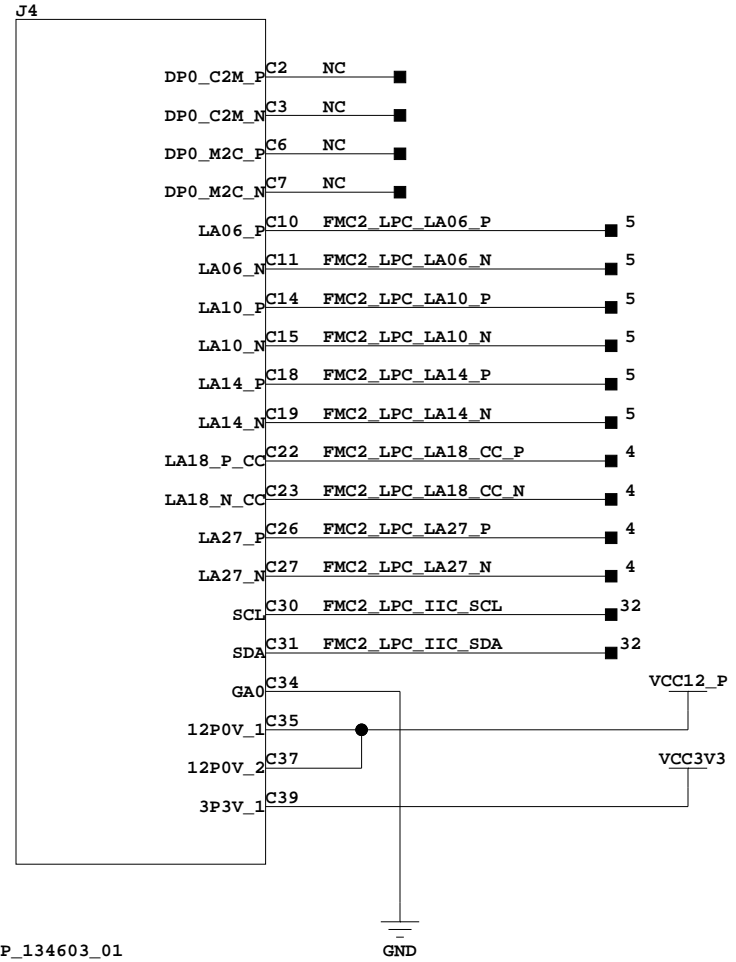


**ANSI/VITA 57.1 - Revised 2010
FMC1 LPC Connector**



Title: ANSI/VITA 57.1 - Revised 2010 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM
 ASSY P/N: 0431696
 PCB P/N: 1280617
 SCH P/N: 0381449

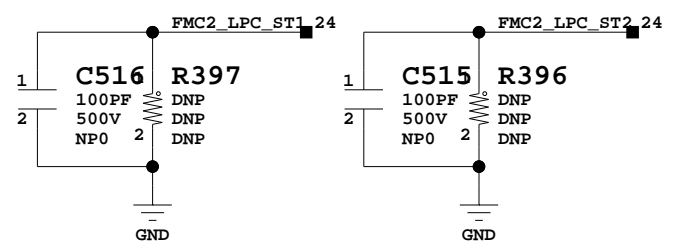
Date:	2-21-2013_17:10	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	23 of 48	Drawn By	BF



ASP_134603_01

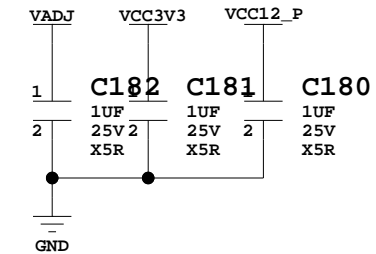
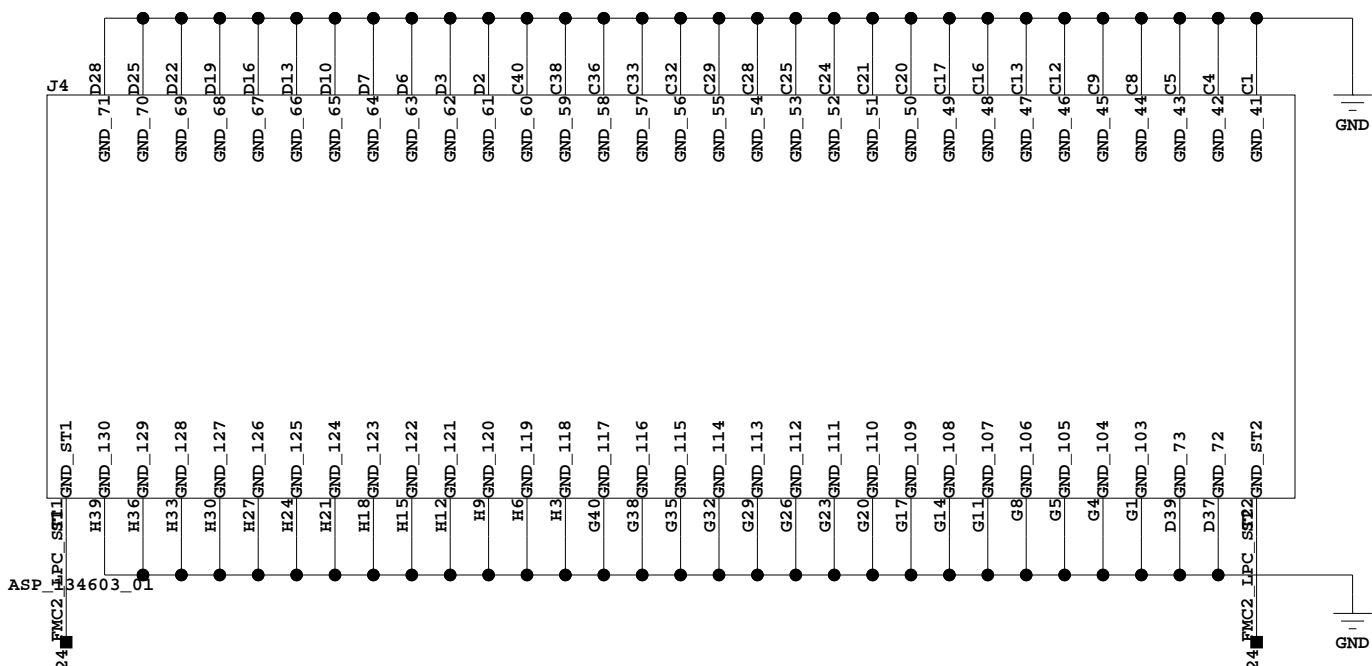
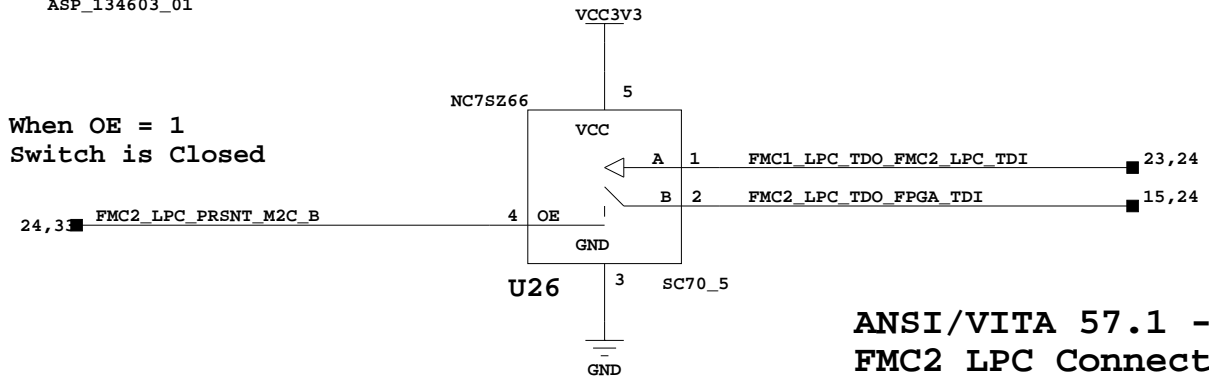
ASP_134603_01

ASP_134603_01



ASP_134603_01

When OE = 1
Switch is Closed



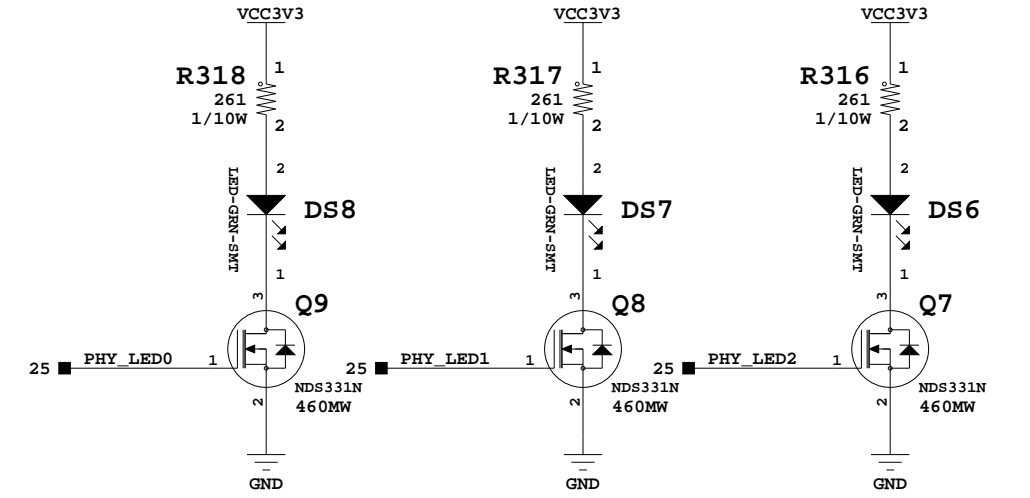
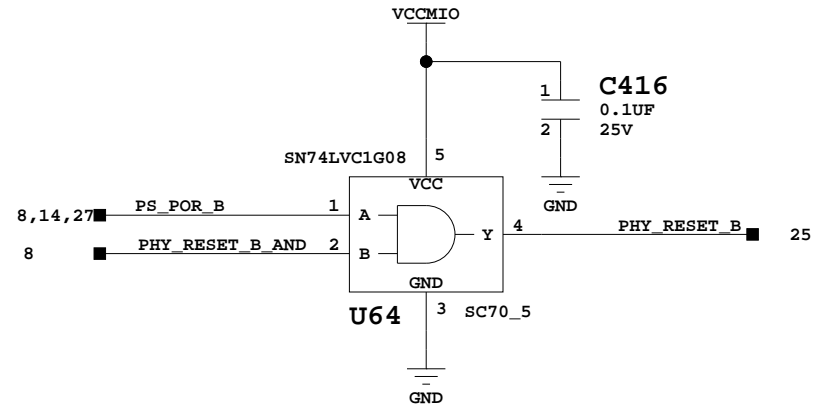
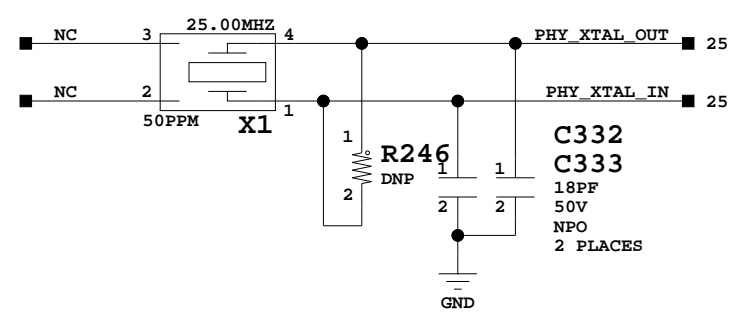
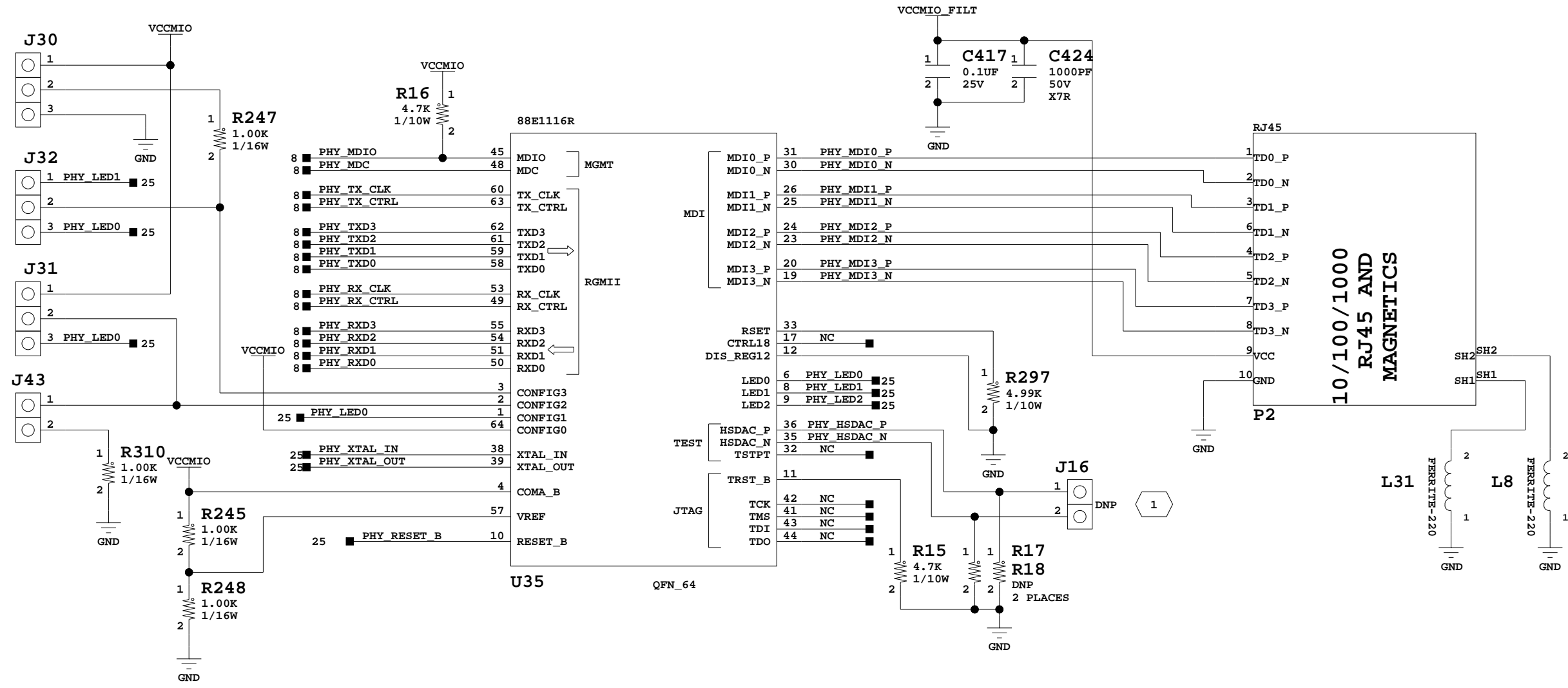
**ANSI/VITA 57.1 - Revised 2010
FMC2 LPC Connector**



Title: ANSI/VITA 57.1 - Revised 2010 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 24 of 48	Drawn By	BF

CONFIGURATION MAPPING

PIN	SETTING	CONFIGURATION
CONFIG0	VCCO_MIO1	PHYAD[1]=1 PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0 PHYAD[2]=1
CONFIG2	GND	ENA_XC=0 PHYAD[4]=0
	EPHY_LED0	ENA_XC=0 PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1 PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0 RGMII_RX=0
	EPHY_LED0	RGMII_TX=0 RGMII_RX=1
	EPHY_LED1	RGMII_TX=1 RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1 RGMII_RX=1



GEM / MDIO

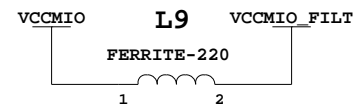
Title: GEM / MDIO SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM
 ASSY P/N: 0431696
 PCB P/N: 1280617
 SCH P/N: 0381449

Date: 2-21-2013_17:10 Ver: 1.1
 Sheet Size: B Rev: 02
 Sheet 25 of 48 Drawn By BF

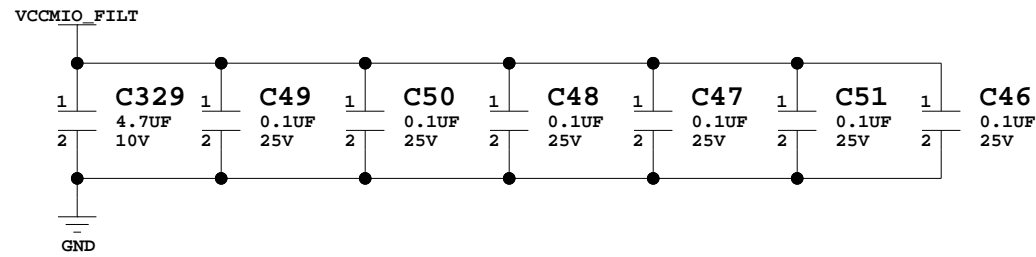
2 SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

1 TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESISTORS ON HSDAC_P AND HSDAC_N.

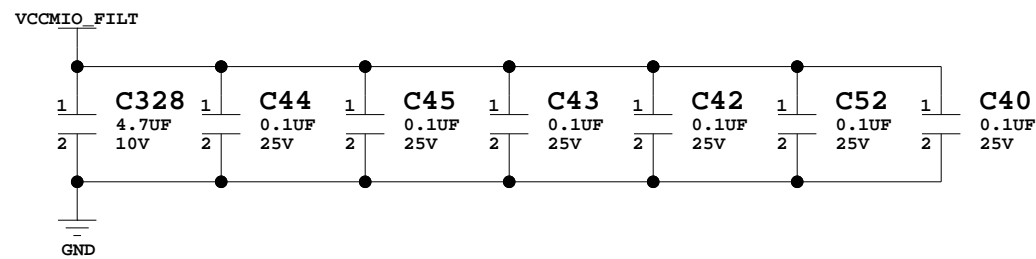
GEM / MDIO - POWER & DECOUPLING



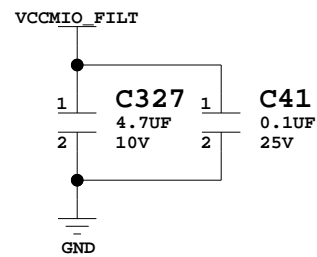
AVDDX, AVDDR, AVDDC



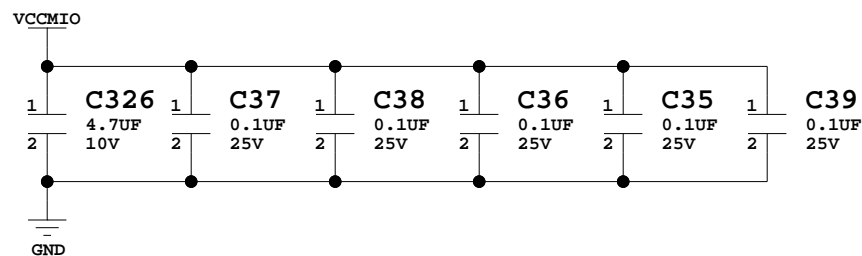
AVDD



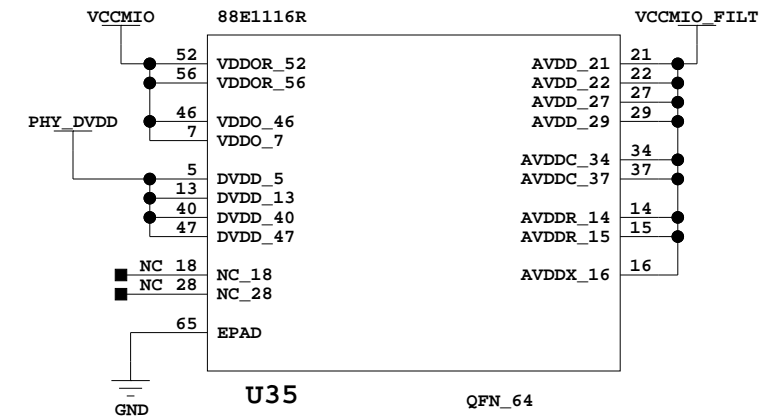
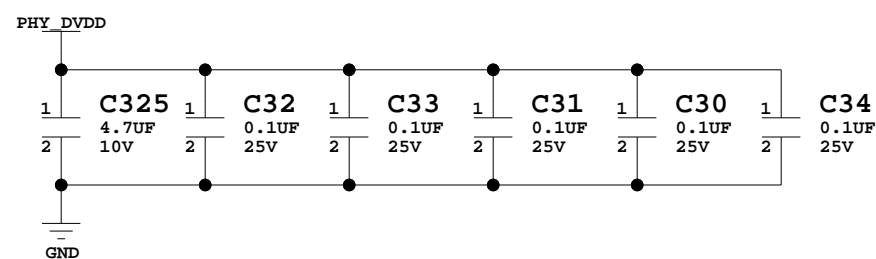
MAGNETICS / RJ45



VDDO, VDDOR



DVDD



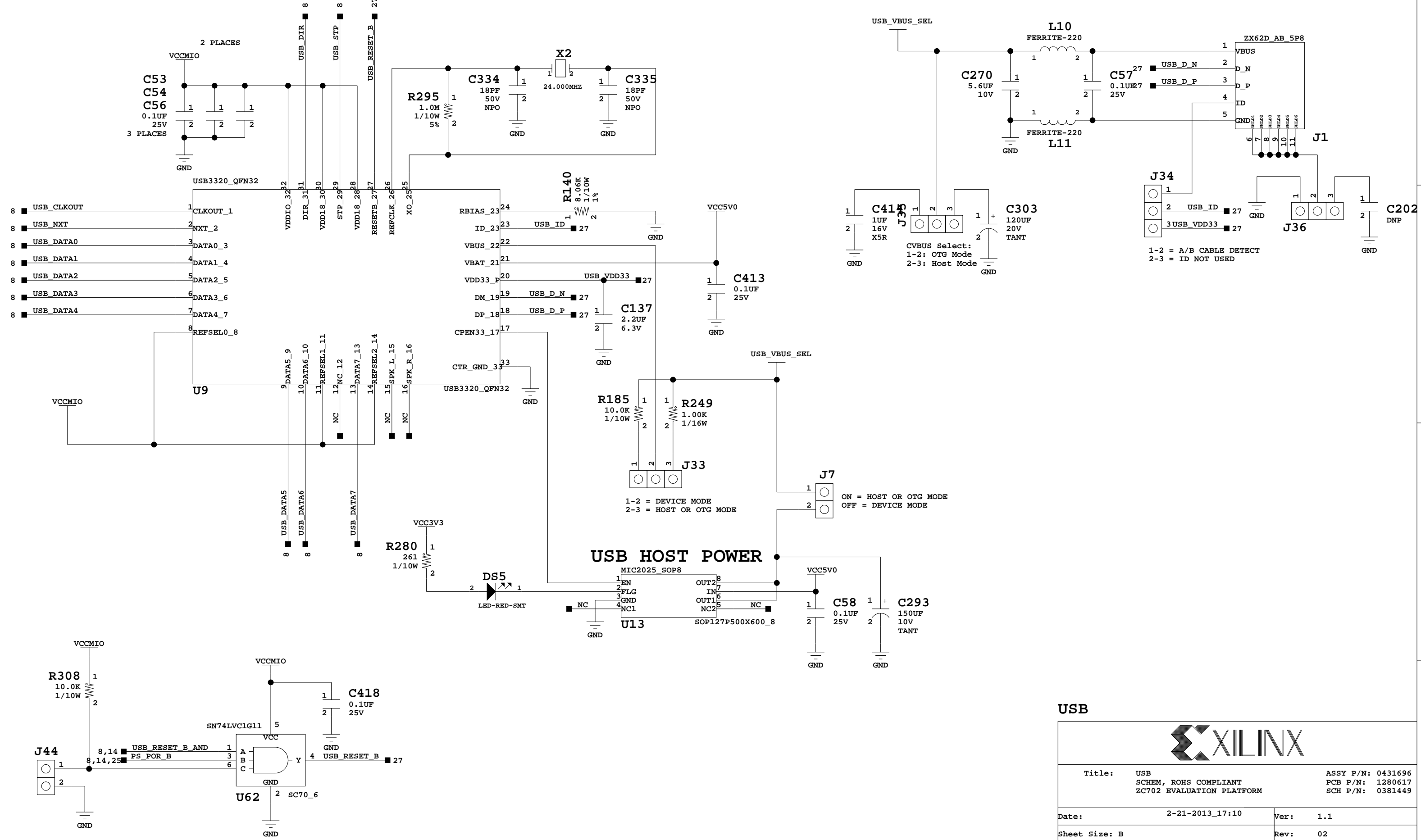
GEM / MDIO



Title: GEM / MDIO SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM
 ASSY P/N: 0431696
 PCB P/N: 1280617
 SCH P/N: 0381449

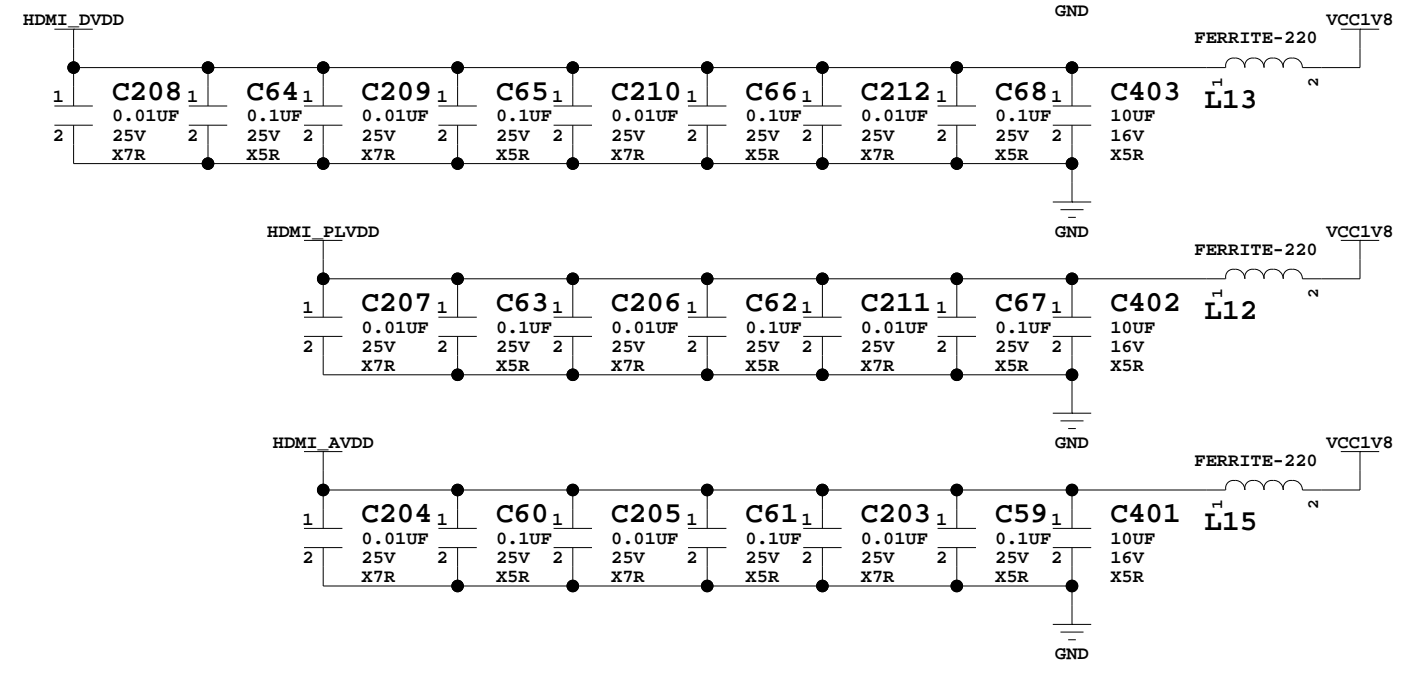
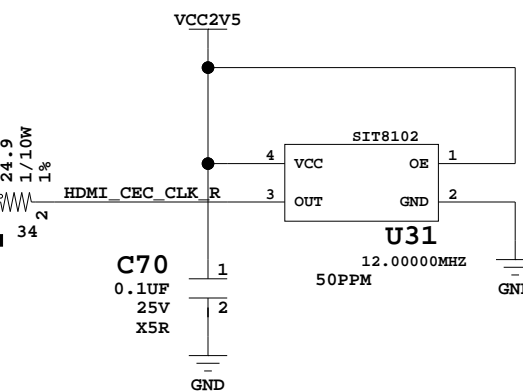
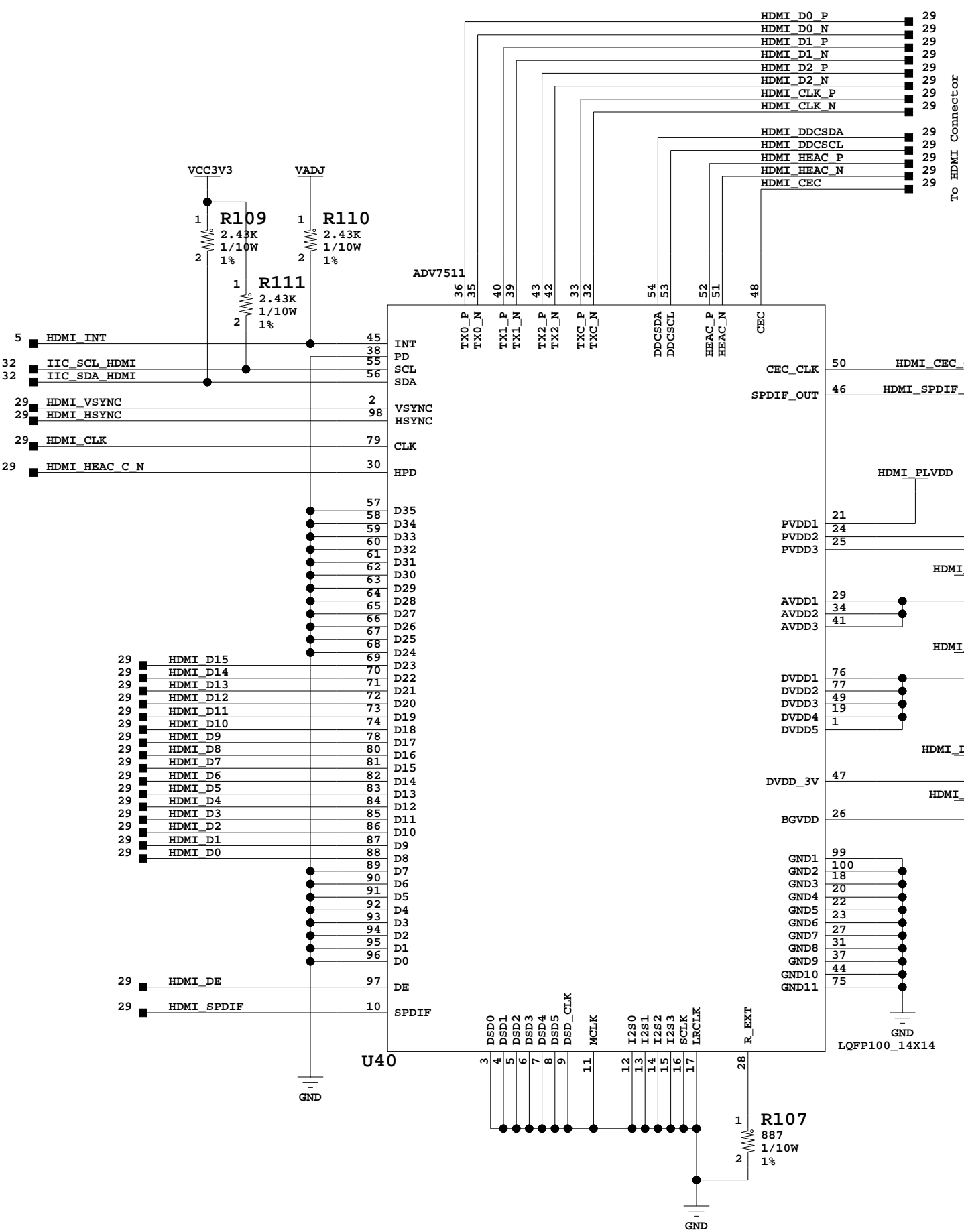
Date: 2-21-2013_17:10 Ver: 1.1
 Sheet Size: B Rev: 02
 Sheet 26 of 48 Drawn By BF

USB 2.0 ULPI TRANSCEIVER AND CONNECTOR



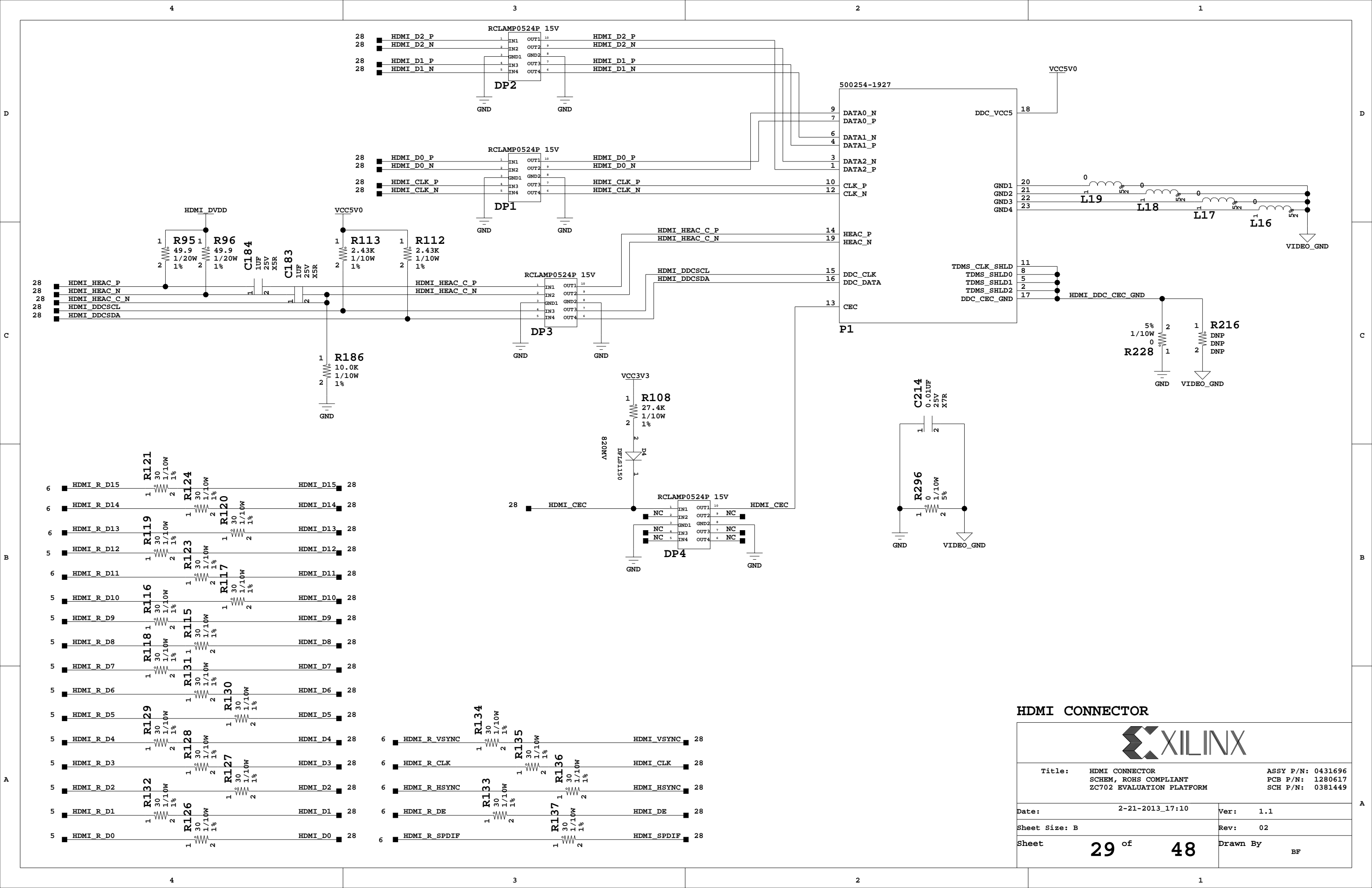
Title: USB SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	
Date: 2-21-2013_17:10	
Ver: 1.1	
Sheet Size: B	
Rev: 02	
Sheet 27 of 48	
Drawn By BF	

ASSY P/N: 0431696
PCB P/N: 1280617
SCH P/N: 0381449



HDMI CODEC

Title: HDMI CODEC SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	
ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
Date: 2-21-2013_17:10	Ver: 1.1
Sheet Size: B	Rev: 02
Sheet 28 of 48	Drawn By BF

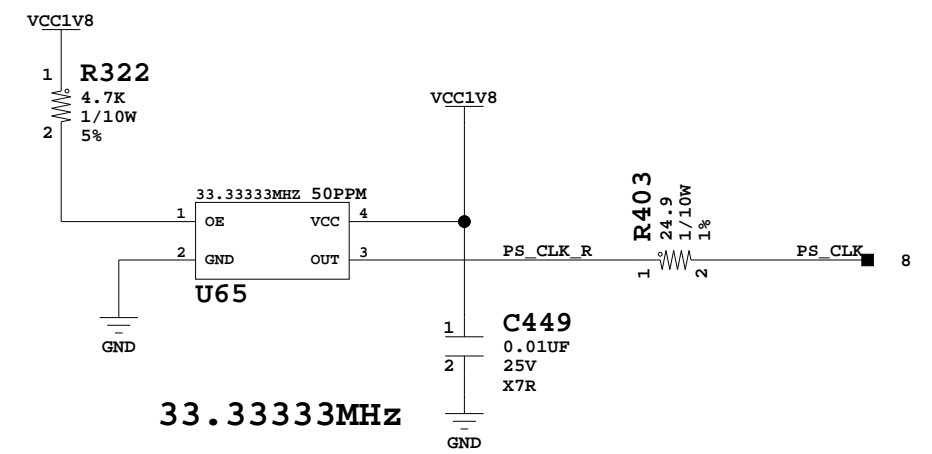
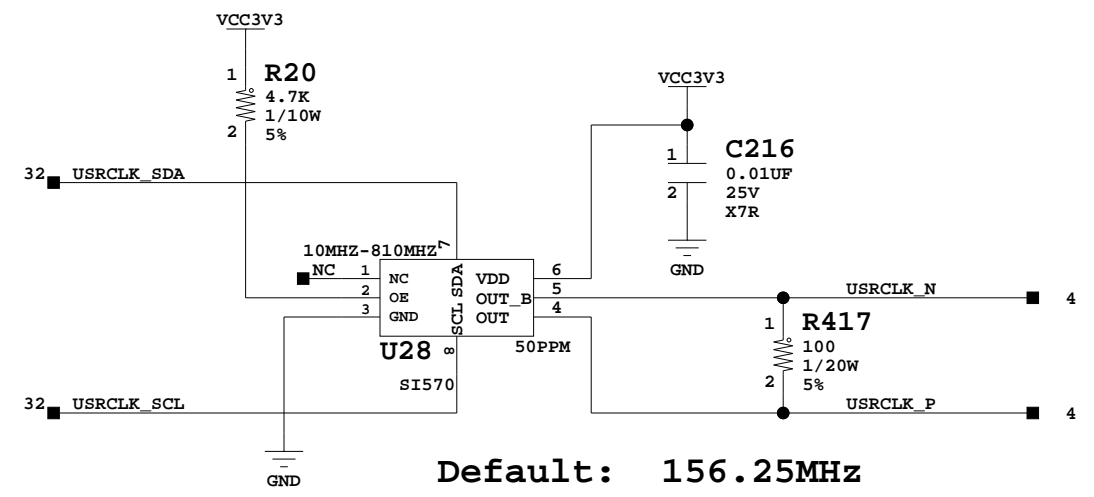
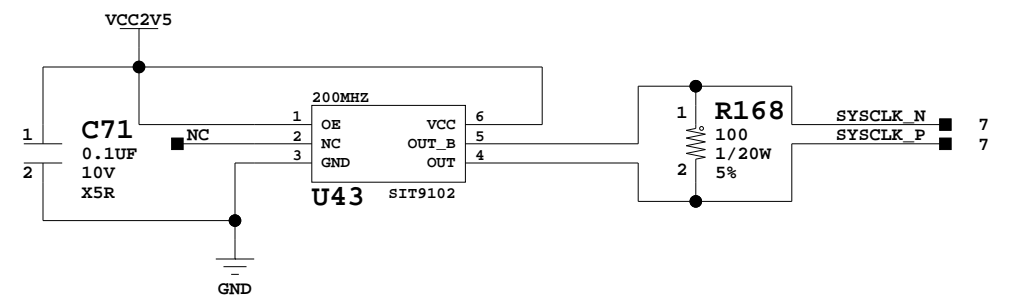


HDMI CONNECTOR



Title: HDMI CONNECTOR SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 29 of 48	Drawn By BF	

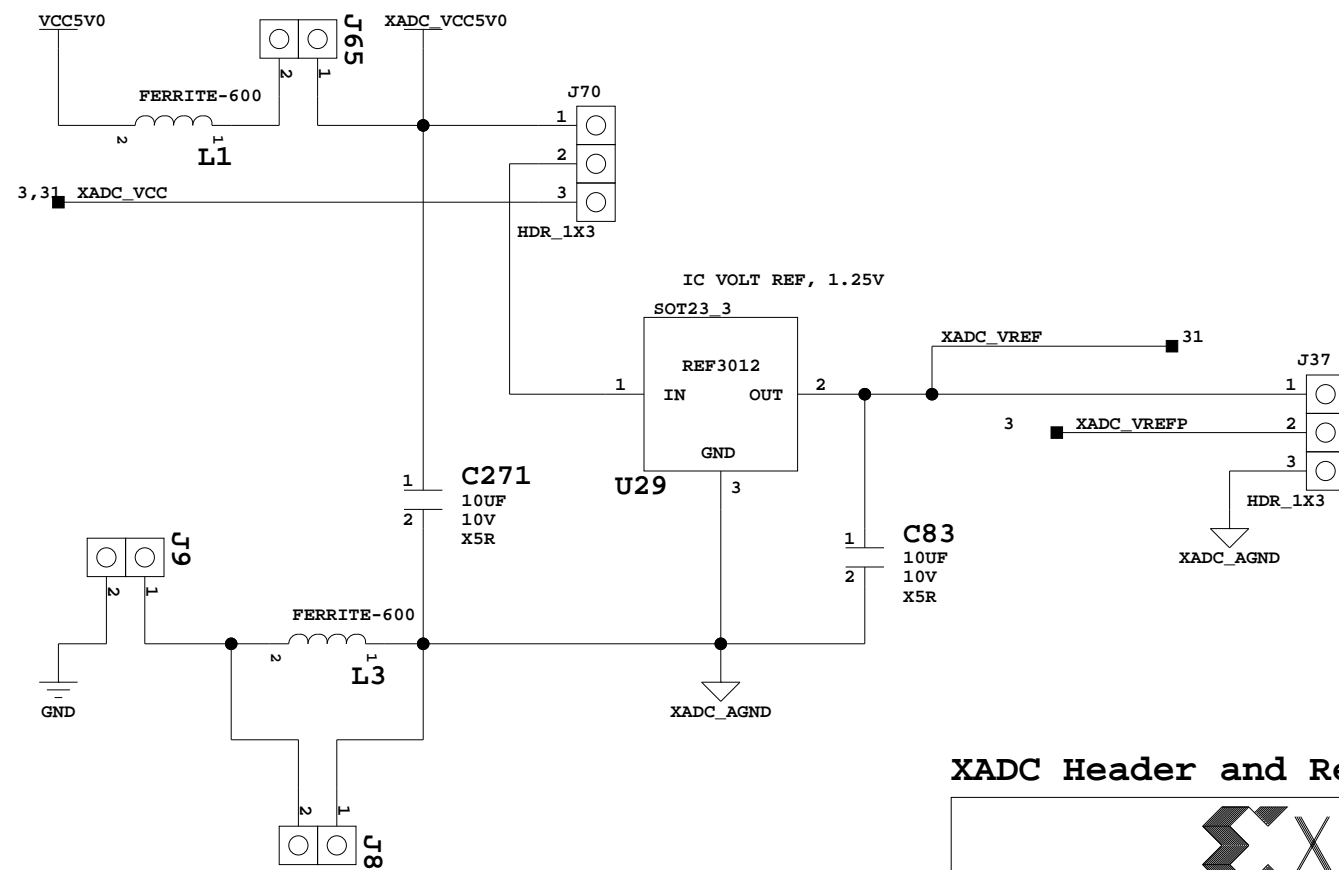
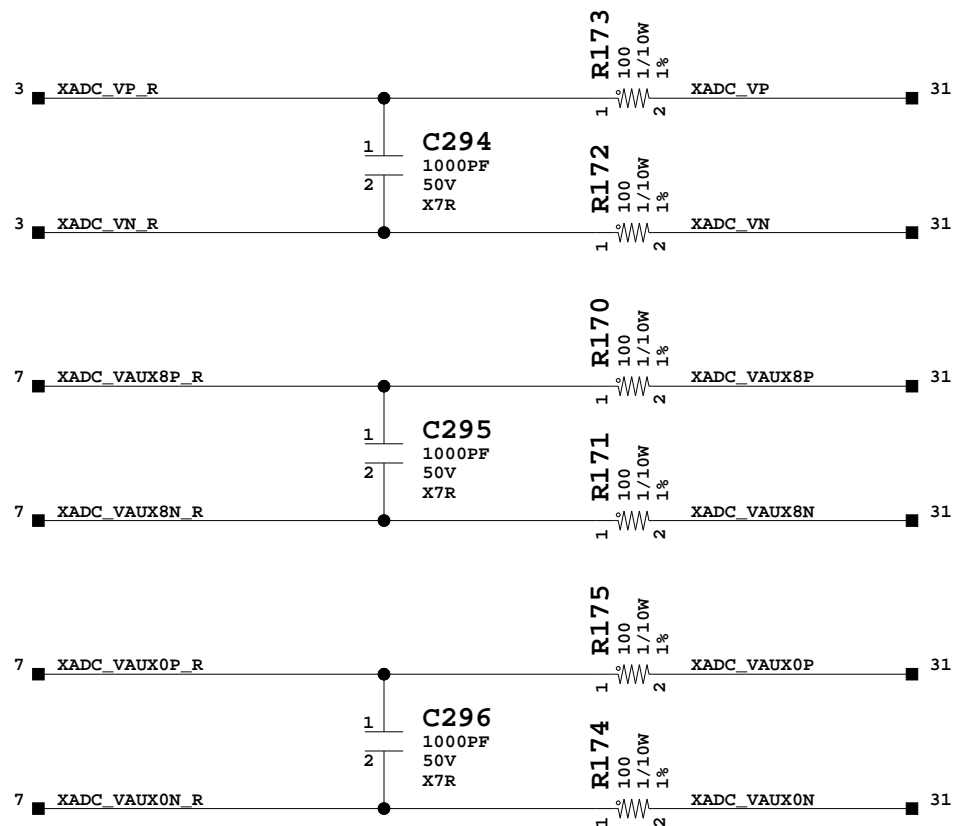
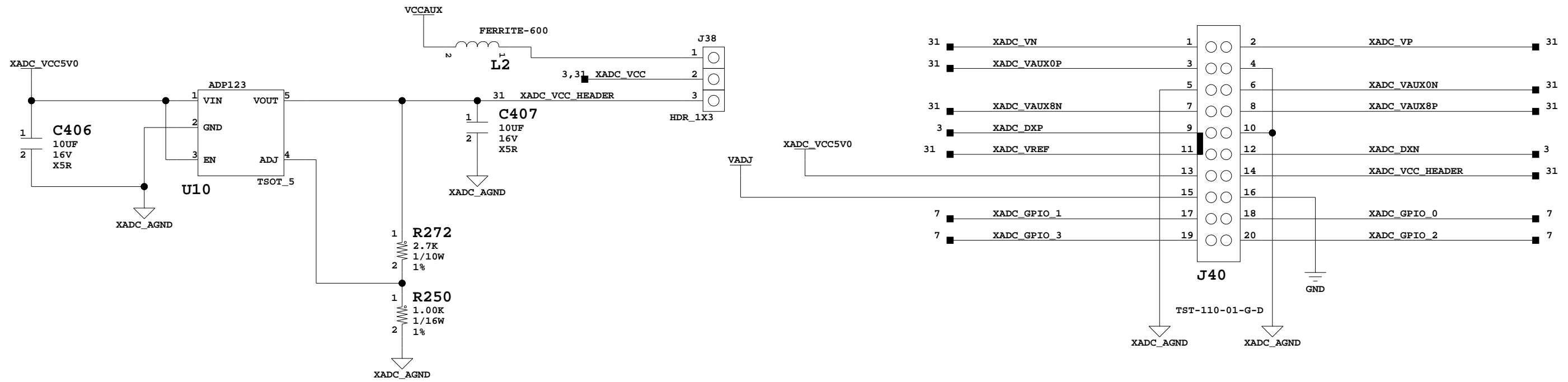
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Clocks



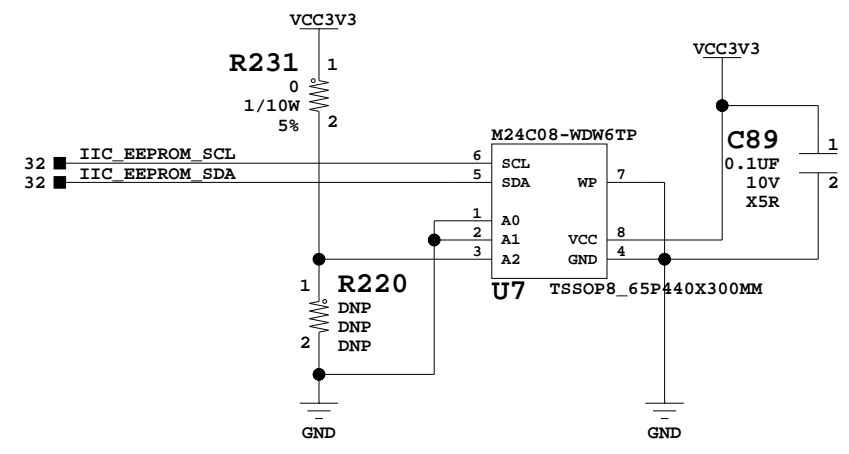
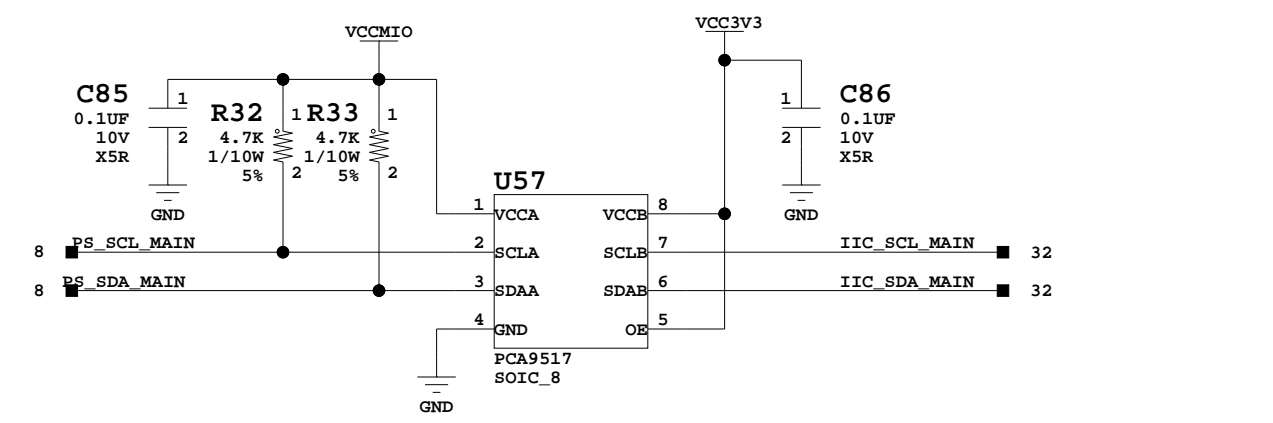
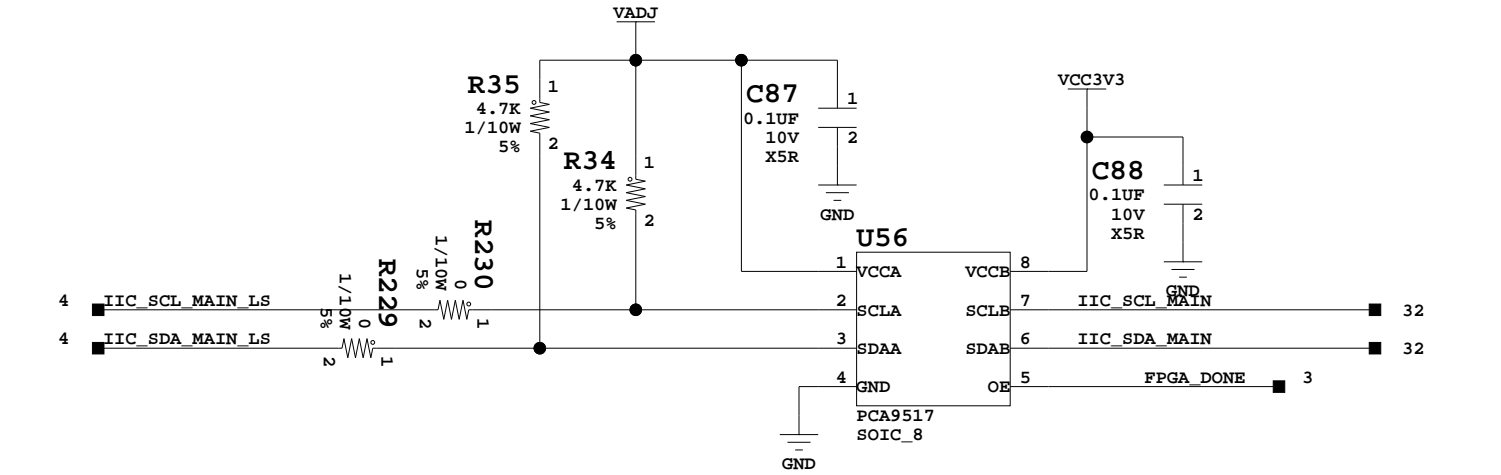
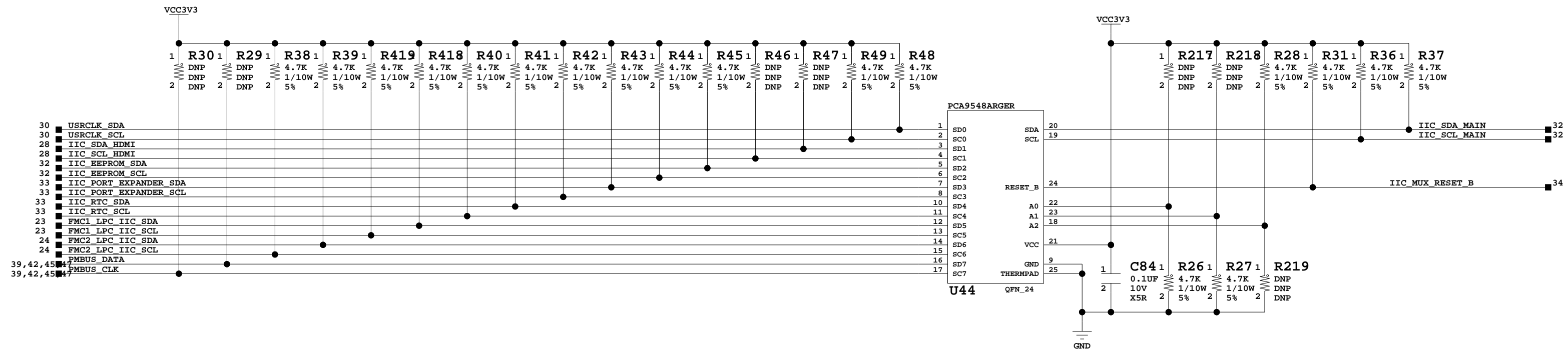
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Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 30 of 48	Drawn By BF	



XADC Header and Reference



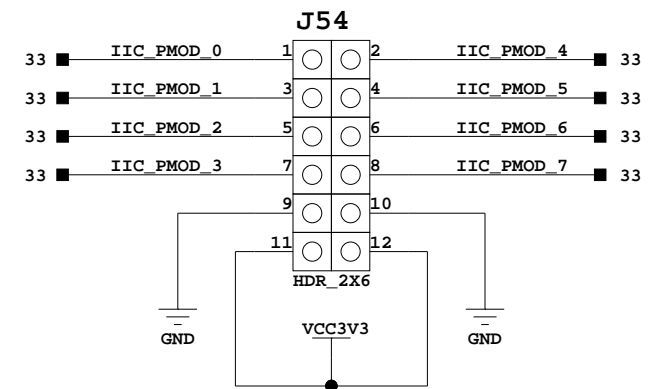
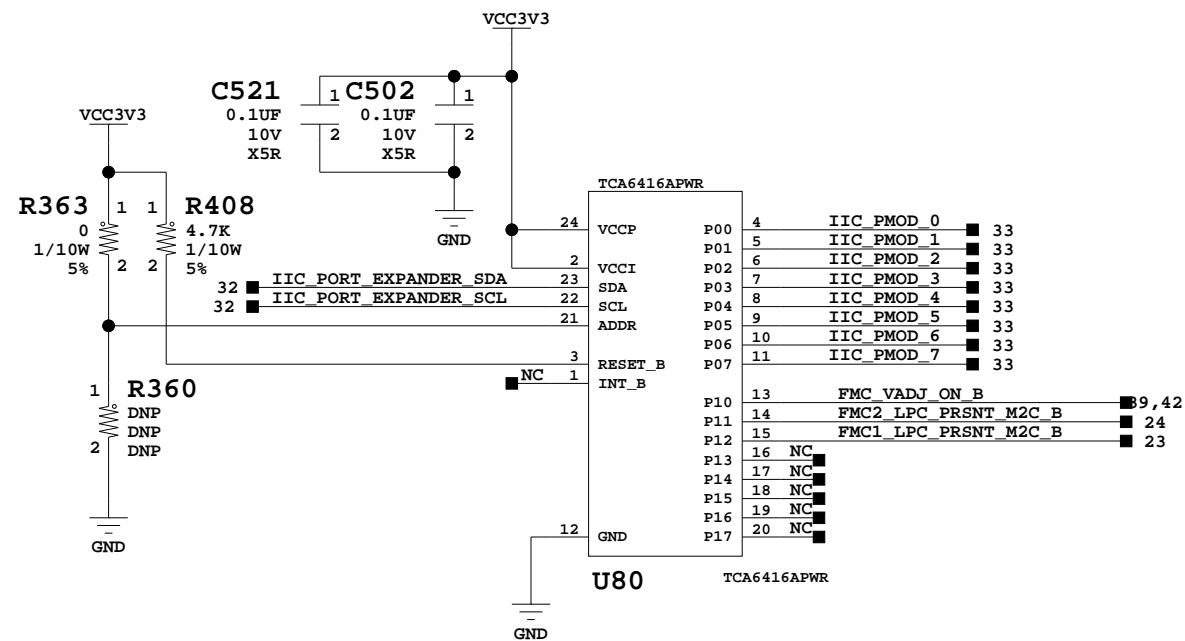
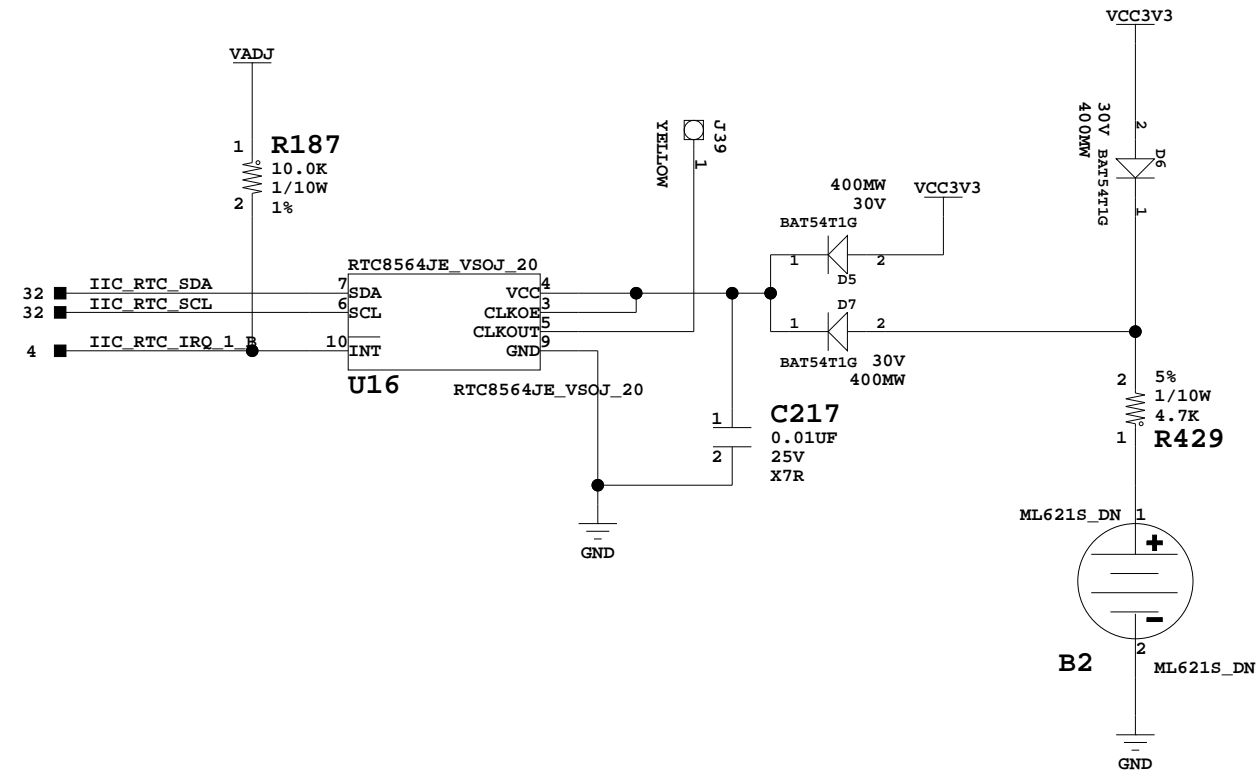
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Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 31 of 48	Drawn By BF	



IIC MUX, EEPROM



Title: IIC MUX, EEPROM SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 32 of 48	Drawn By BF	



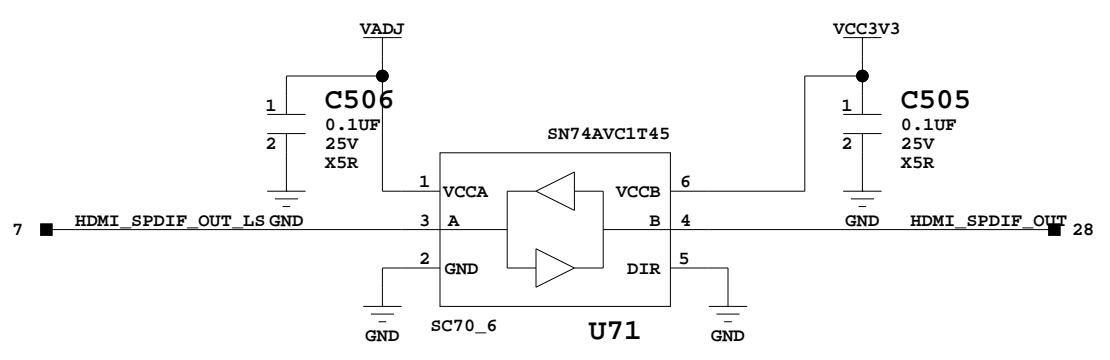
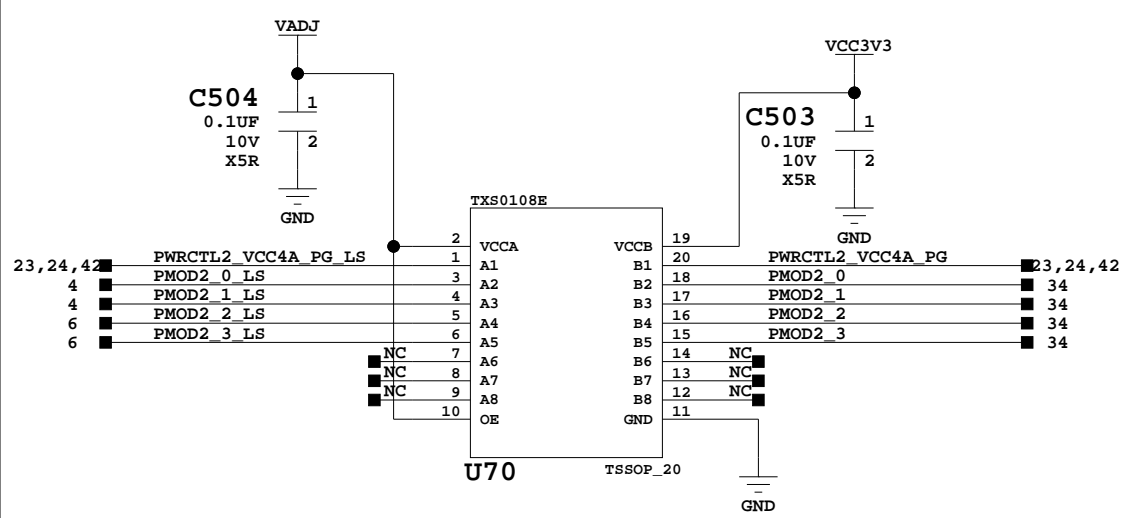
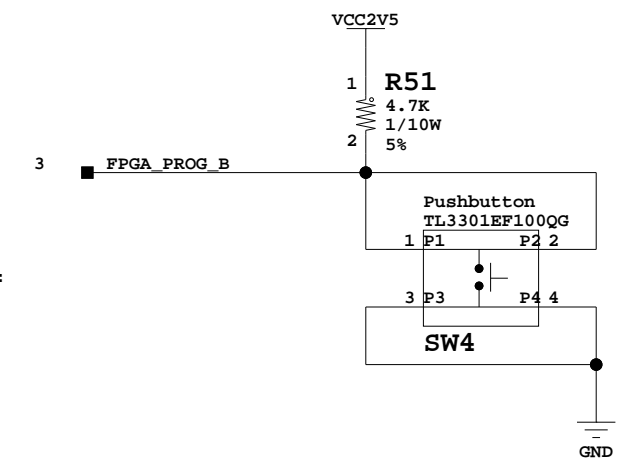
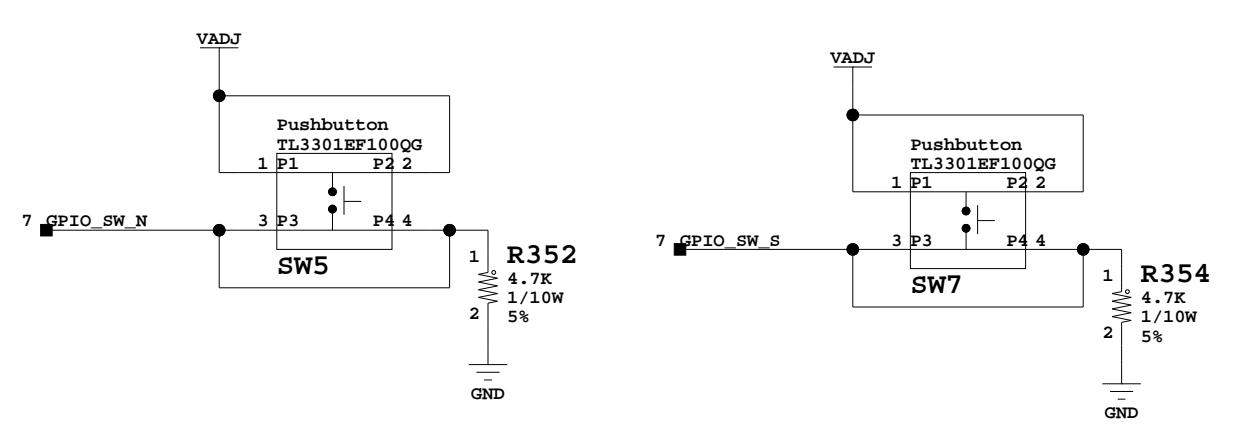
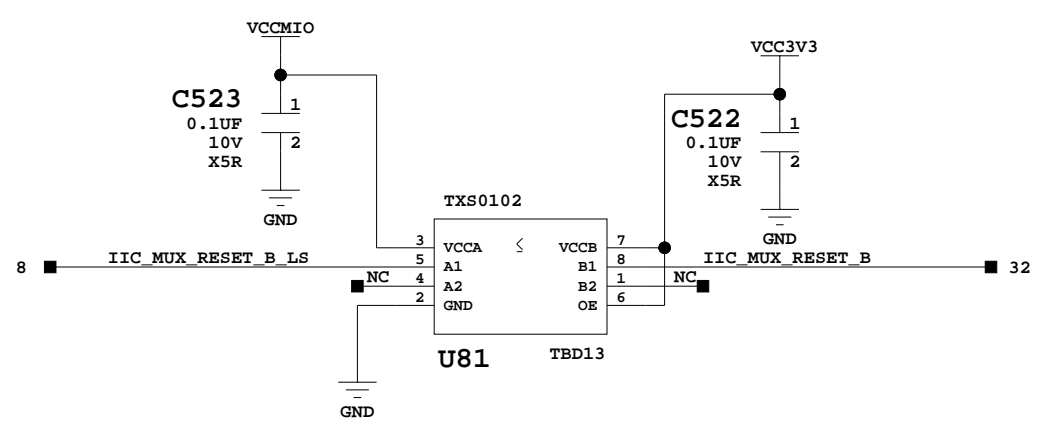
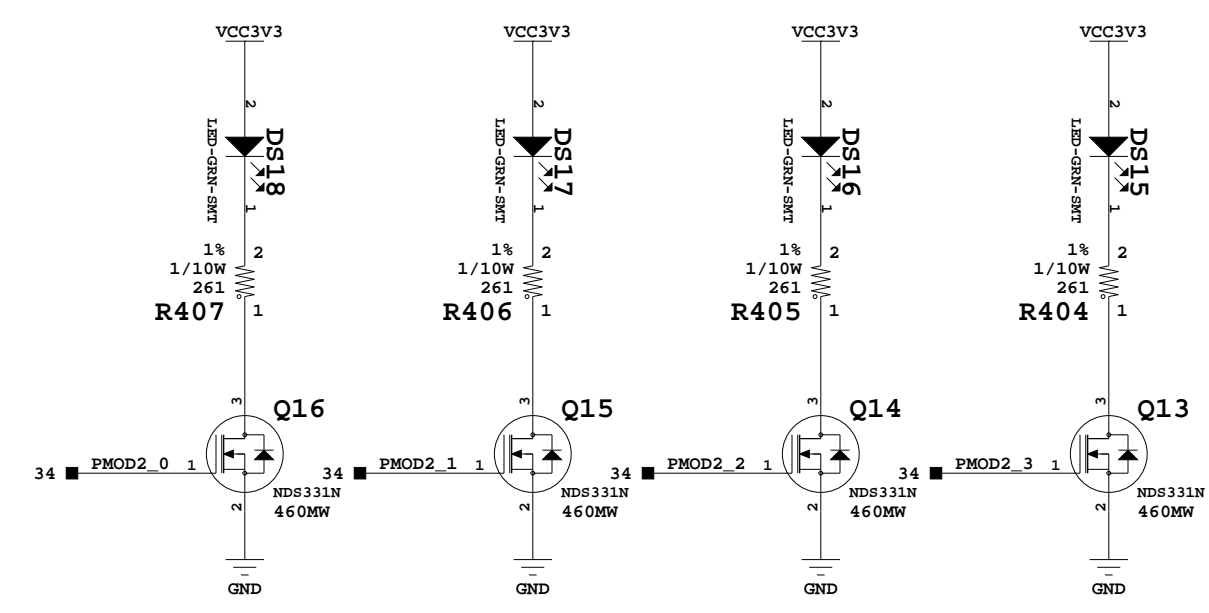
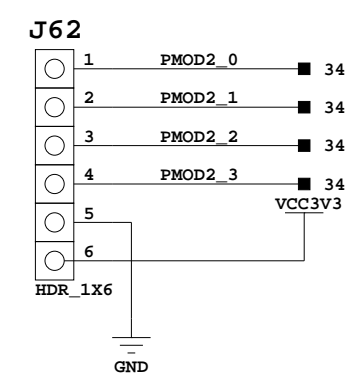
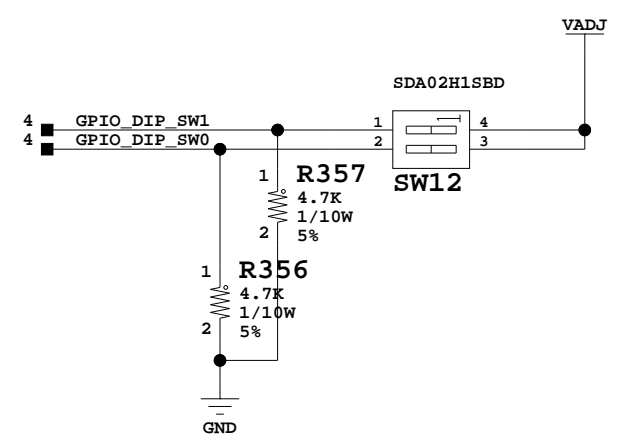
IIC Real Time Clock, Port Expander



Title: IIC Real Time Clock, Port Expander
SCHEM, ROHS COMPLIANT
ZC702 EVALUATION PLATFORM

ASSY P/N: 0431696
PCB P/N: 1280617
SCH P/N: 0381449

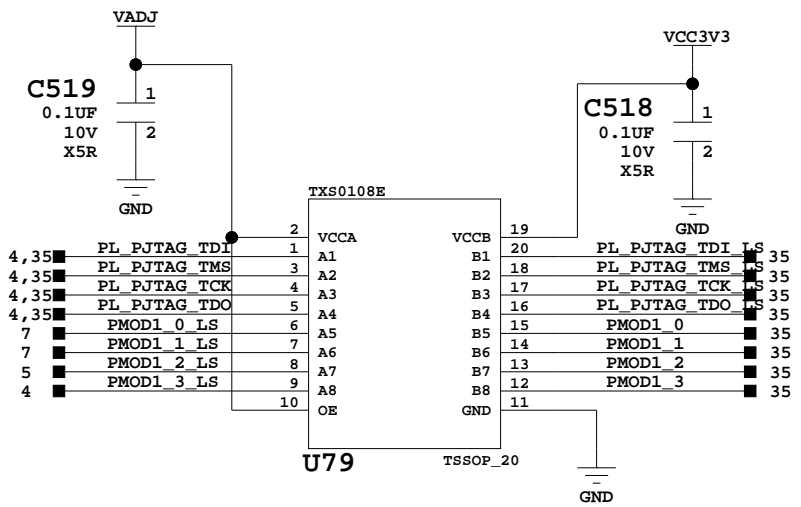
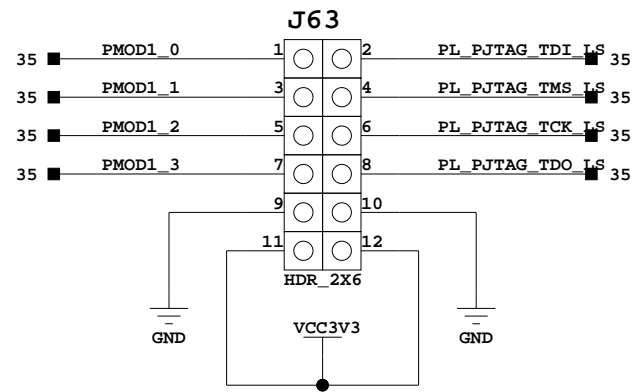
Date:	2-21-2013_17:10	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	33 of 48	Drawn By	BF



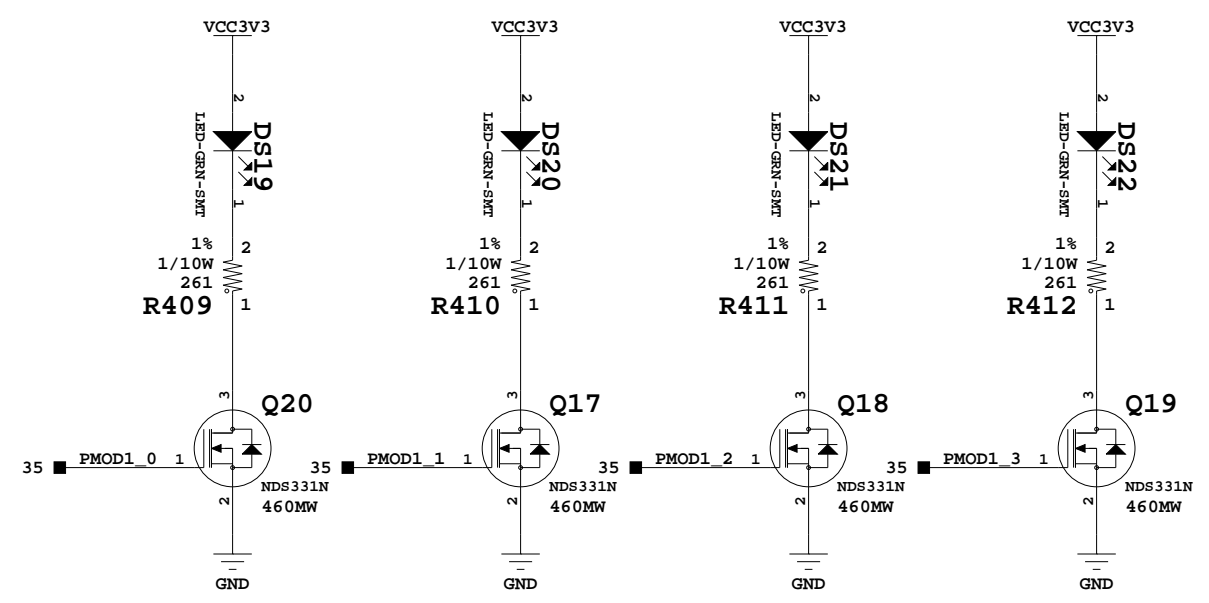
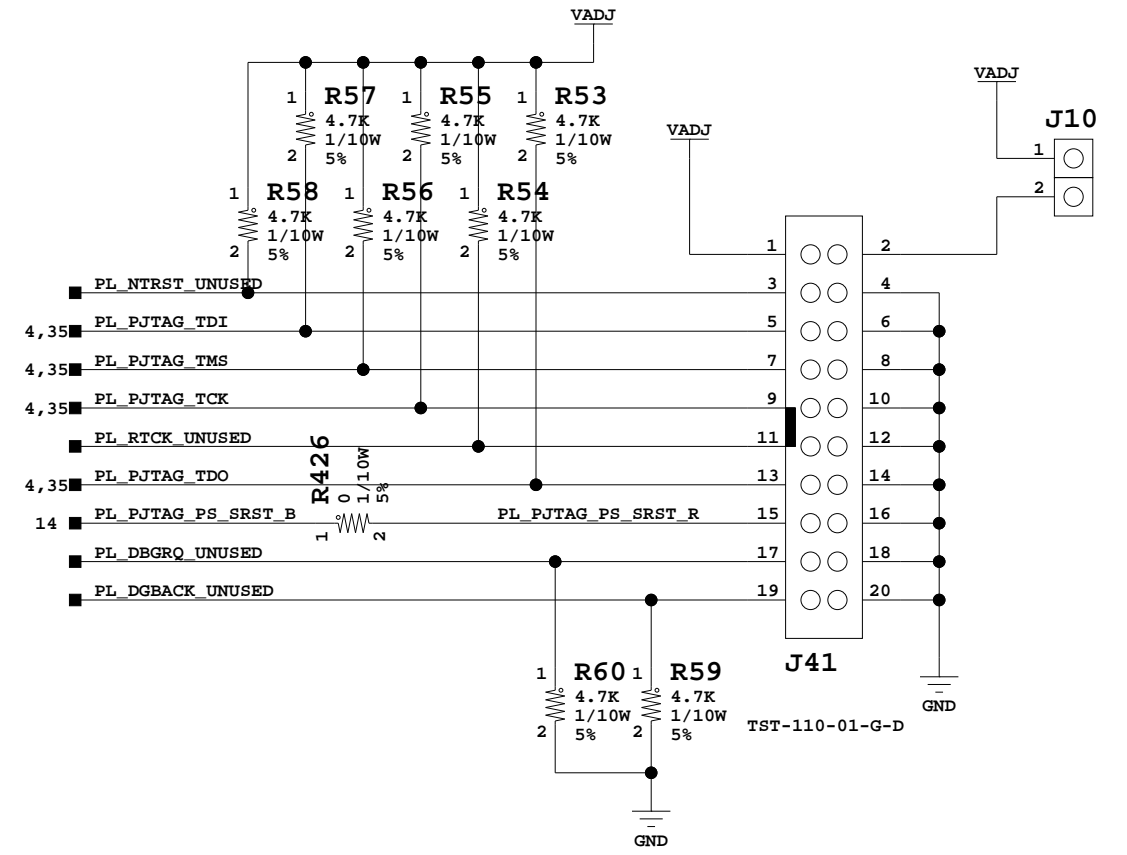
GPIO, Level Shifters, PMOD2



Title: GPIO, Level Shifters, PMOD2 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 34 of 48	Drawn By	BF



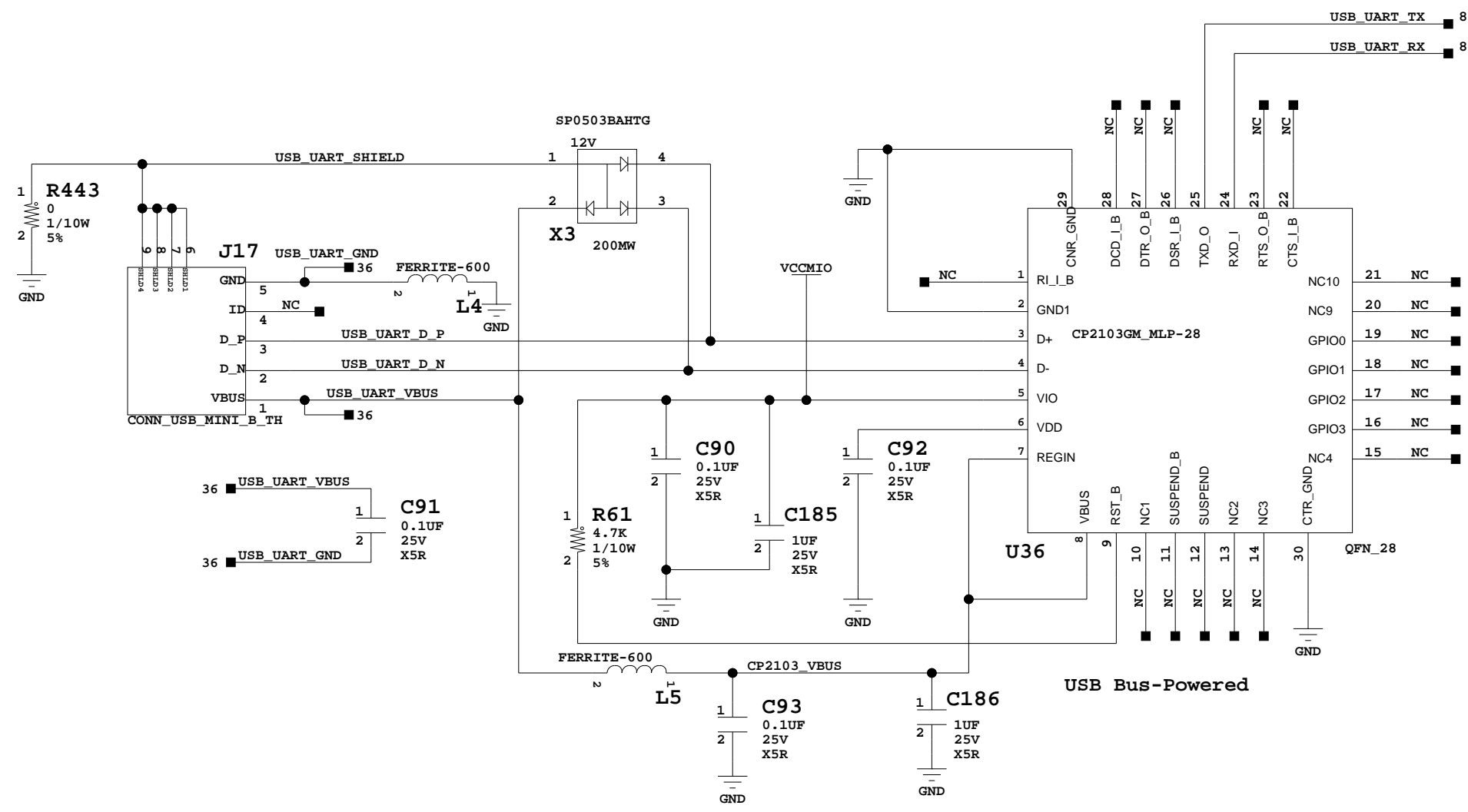
ARM PJTAG Header



ARM PJTAG Header, PMOD1



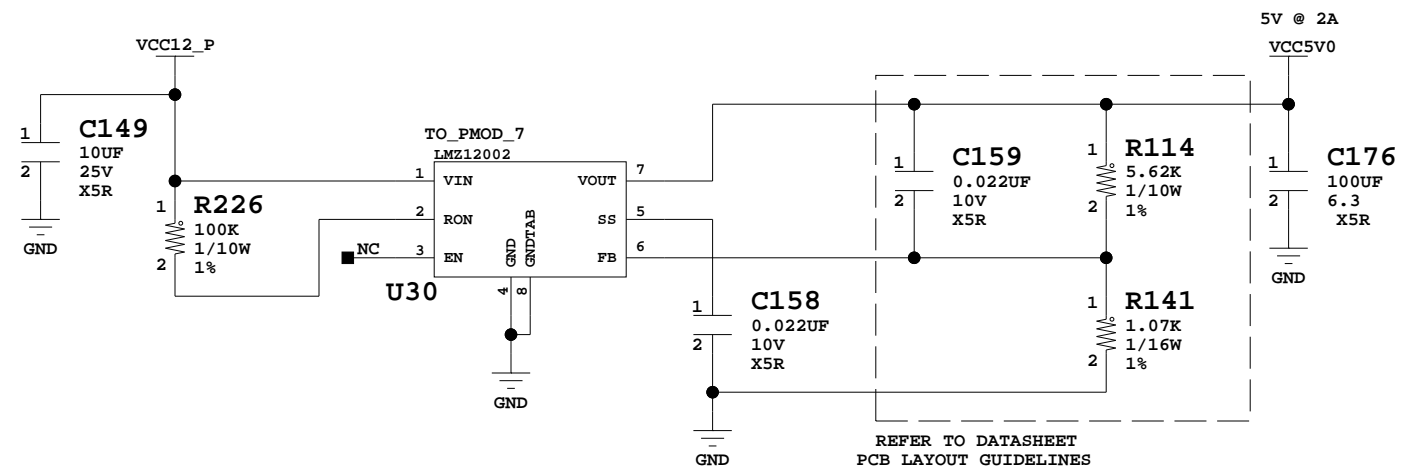
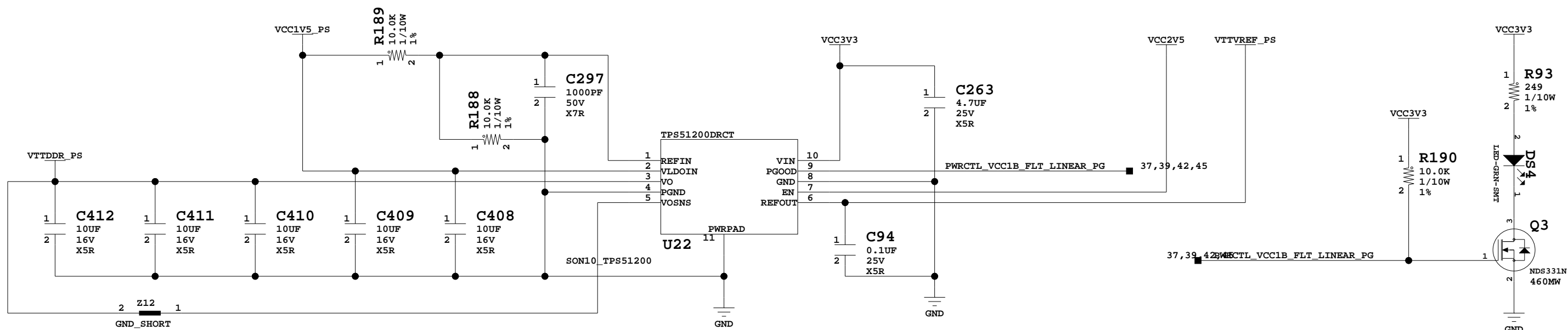
Title: ARM PJTAG Header, PMOD1 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 35 of 48	Drawn By BF	



USB UART



Title: USB UART SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date:	2-21-2013_17:10	Ver: 1.1
Sheet Size:	B	Rev: 02
Sheet	36 of 48	Drawn By BF



Linear Power Supplies		
Title:	Linear Power Supplies SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date:	2-21-2013_17:10	Ver: 1.1
Sheet Size:	B	Rev: 02
Sheet	37 of 48	Drawn By BF

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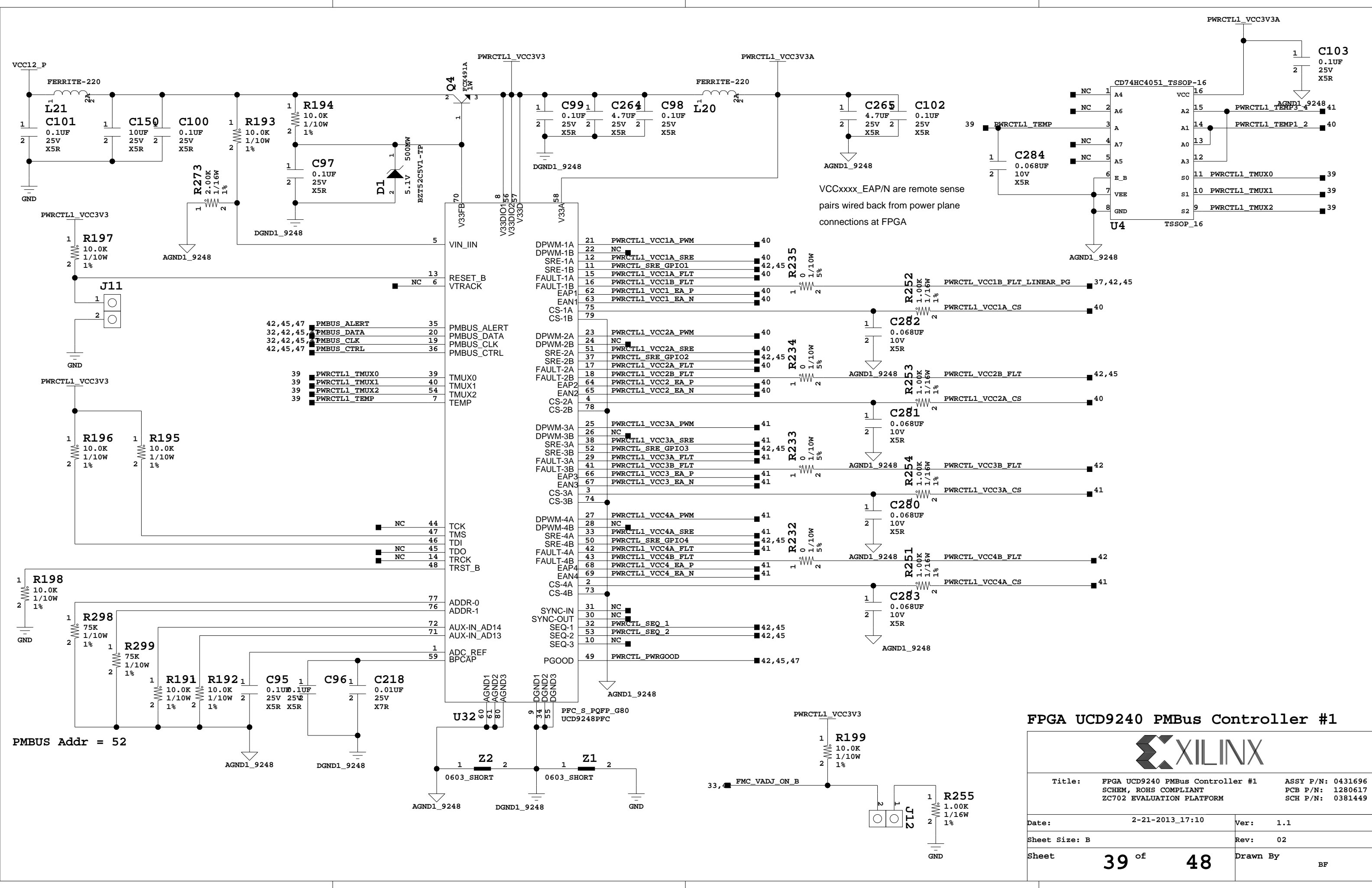


Title:	Blank Page SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
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Date:	2-21-2013_17:10	Ver:	1.1
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Sheet Size:	B	Rev:	02
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Sheet	38 of 48	Drawn By	BF
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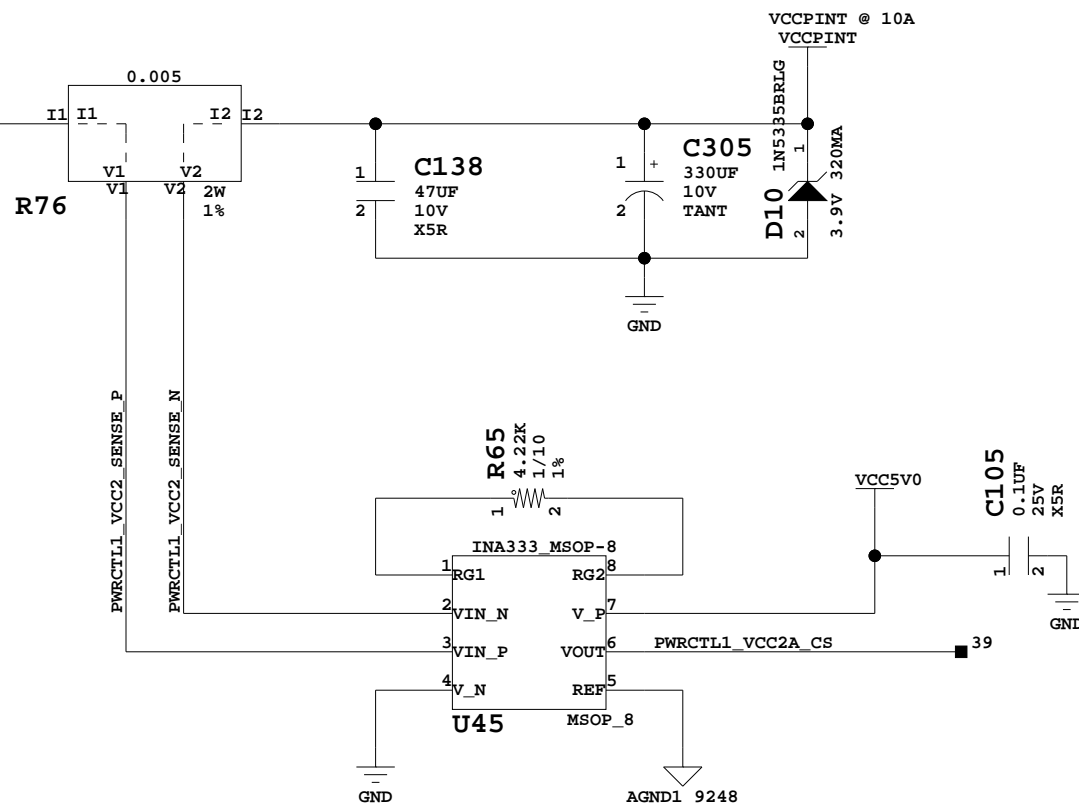
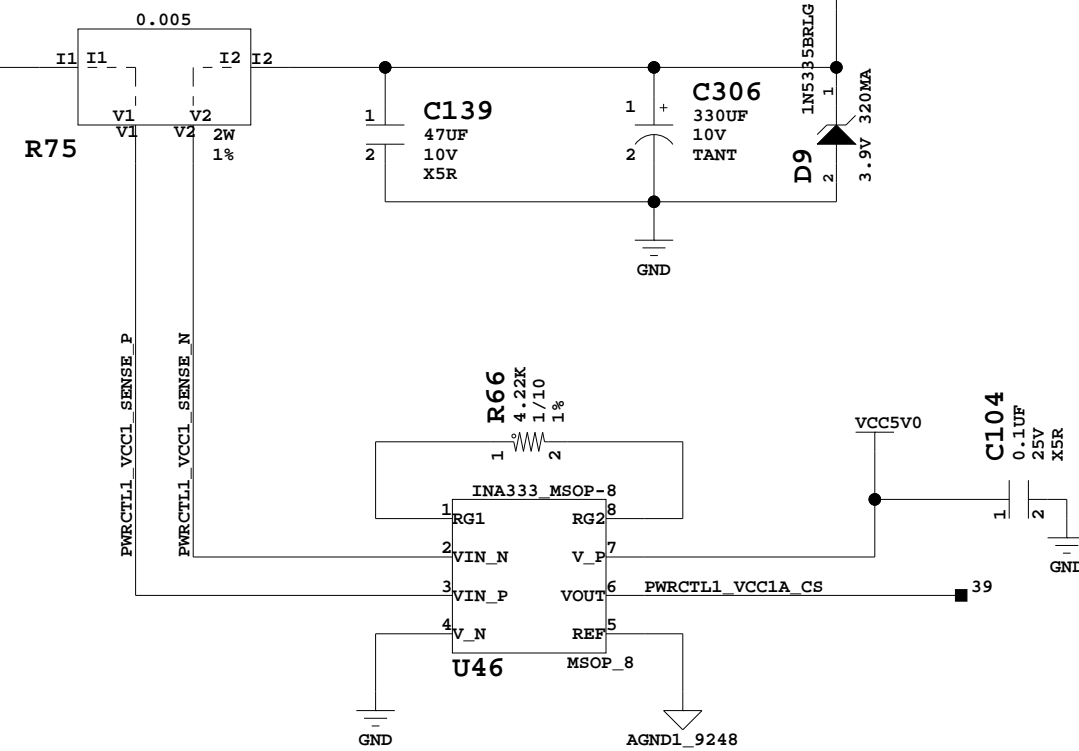
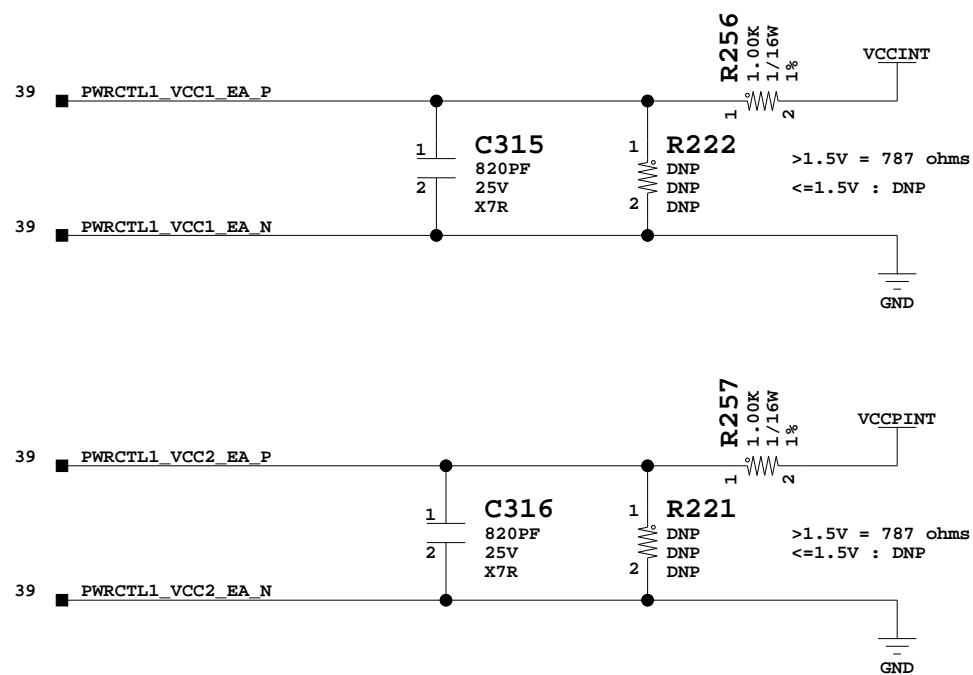
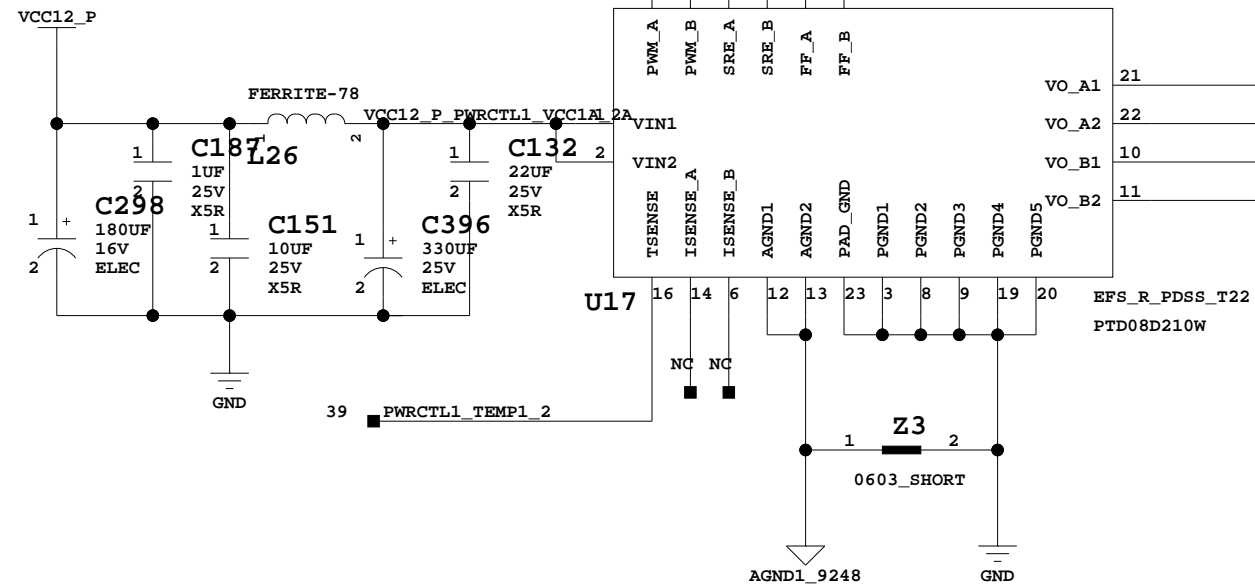
FPGA UCD9240 PMBus Controller #1



Title: FPGA UCD9240 PMBus Controller #1 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 39 of 48	Drawn By BF	

PMBUS Addr = 52

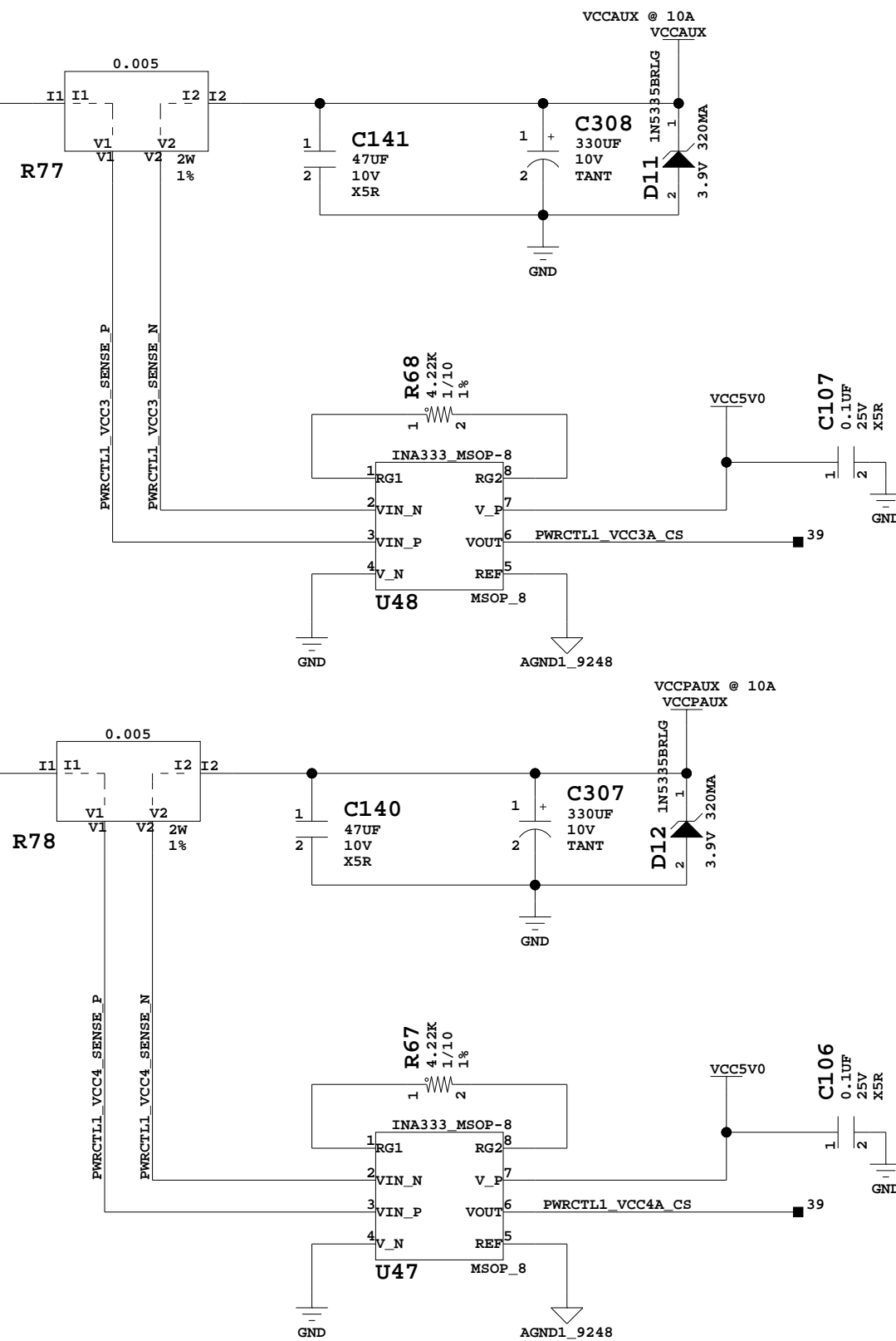
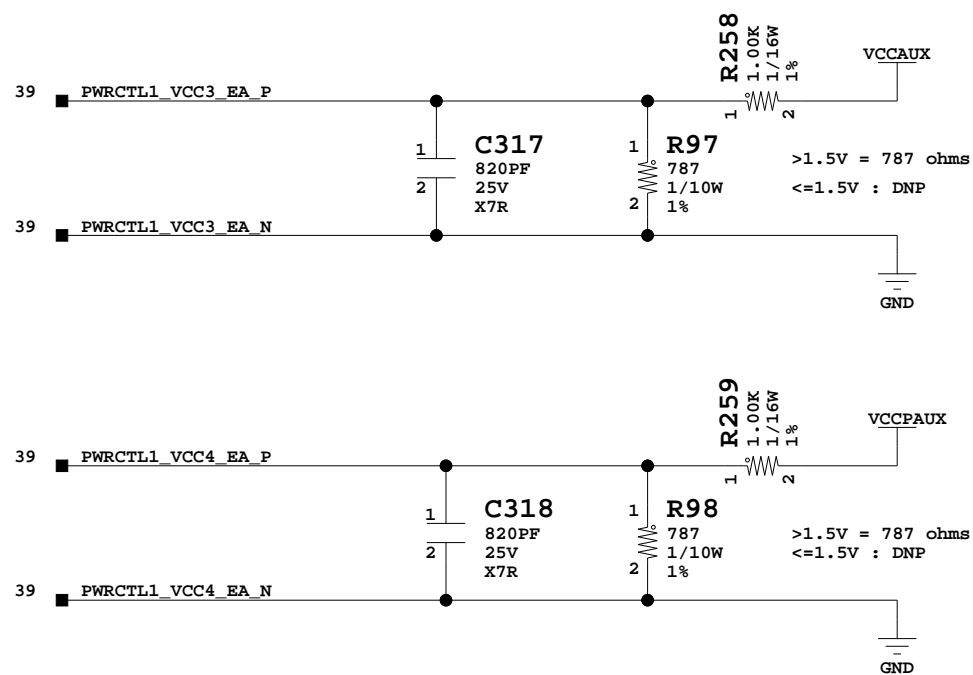
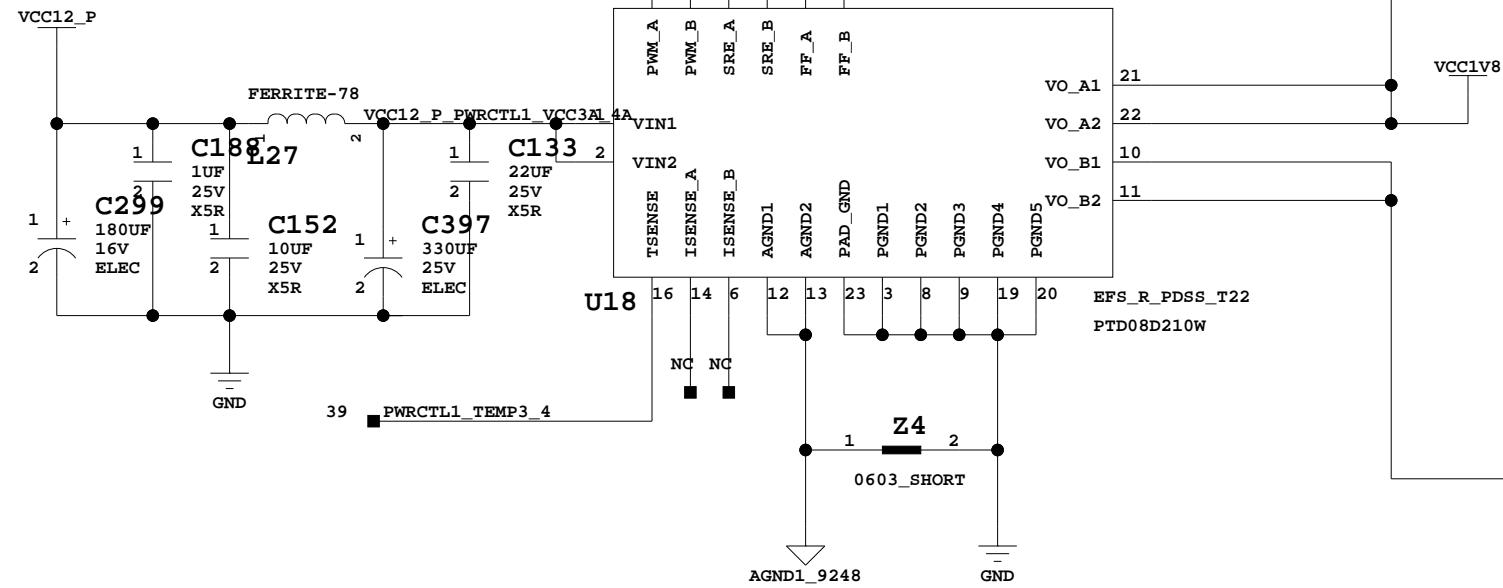
VCCxxx_EAP/N are remote sense pairs wired back from power plane connections at FPGA



Dual 10A Max. Power Channels



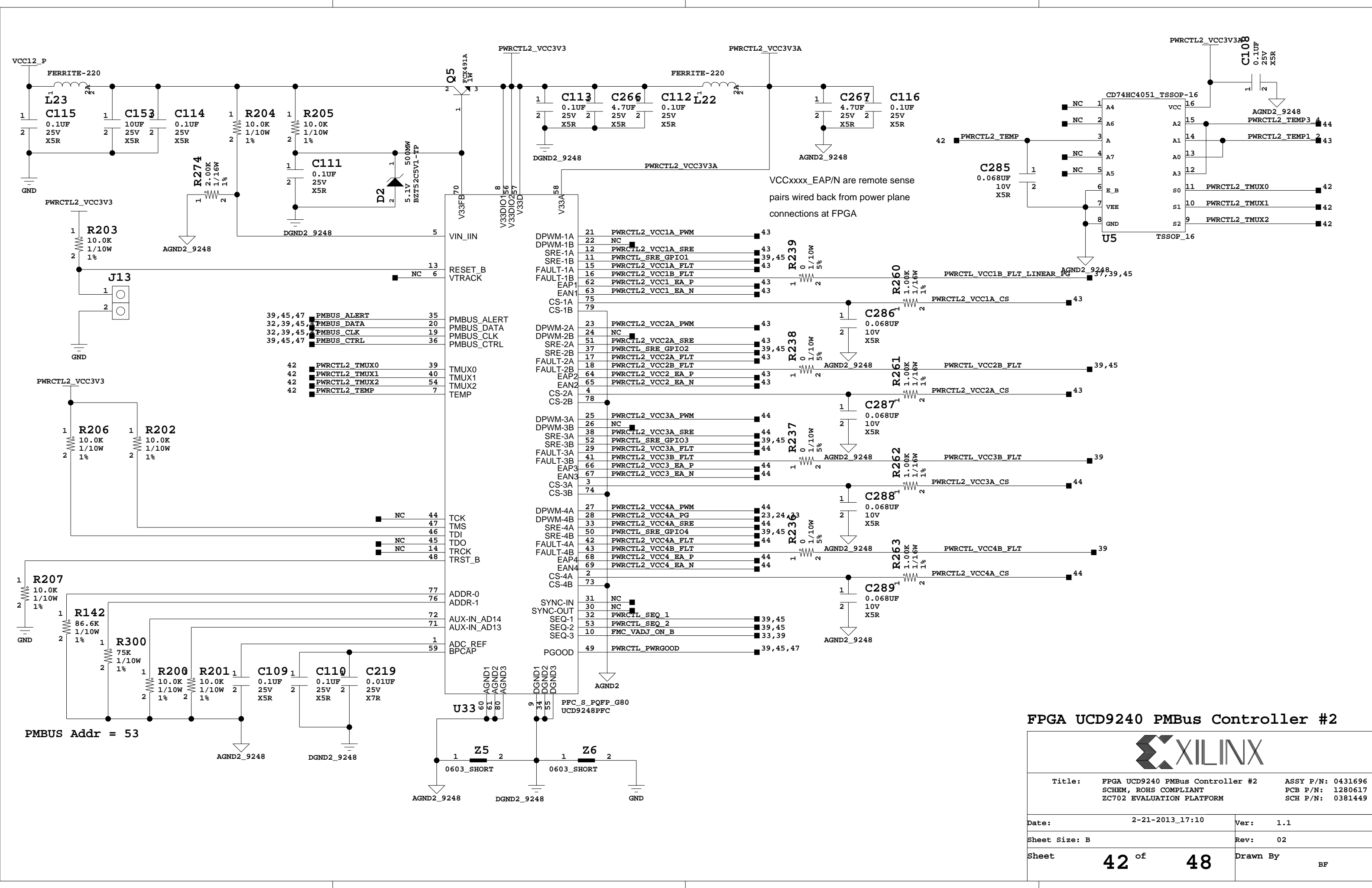
Title: Dual 10A Max. Power Channels		ASSY P/N: 0431696
SCHEM, ROHS COMPLIANT		PCB P/N: 1280617
ZC702 EVALUATION PLATFORM		SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 40 of 48	Drawn By BF	




Dual 10A Max. Power Channels



Title: Dual 10A Max. Power Channels		ASSY P/N: 0431696
SCHEM, ROHS COMPLIANT		PCB P/N: 1280617
ZC702 EVALUATION PLATFORM		SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 41 of 48	Drawn By BF	



FPGA UCD9240 PMBus Controller #2

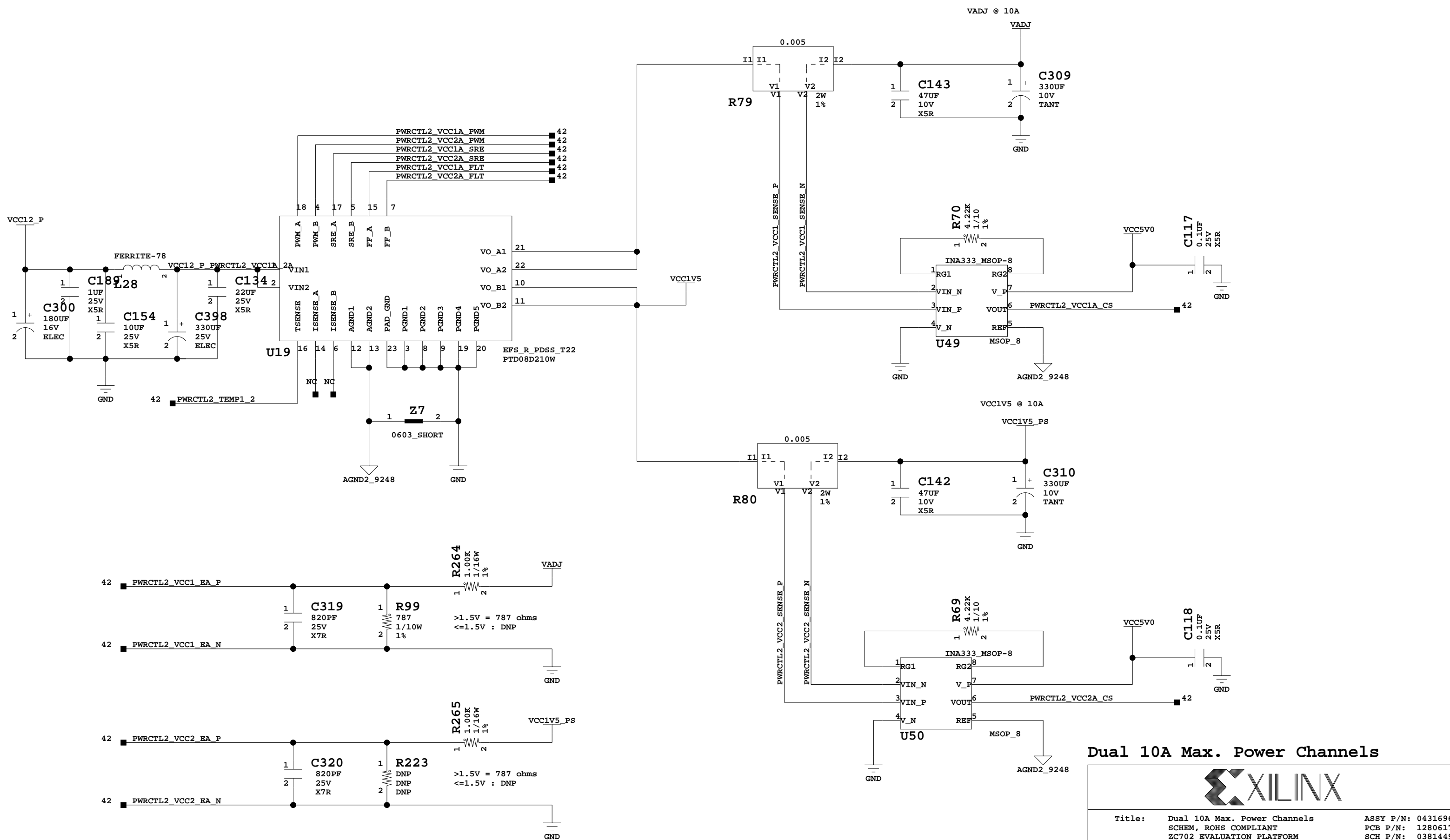


Title: FPGA UCD9240 PMBus Controller #2		ASSY P/N: 0431696
SCHEM, ROHS COMPLIANT		PCB P/N: 1280617
ZC702 EVALUATION PLATFORM		SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 42 of 48	Drawn By BF	

VCCxxxx_EAP/N are remote sense pairs wired back from power plane connections at FPGA

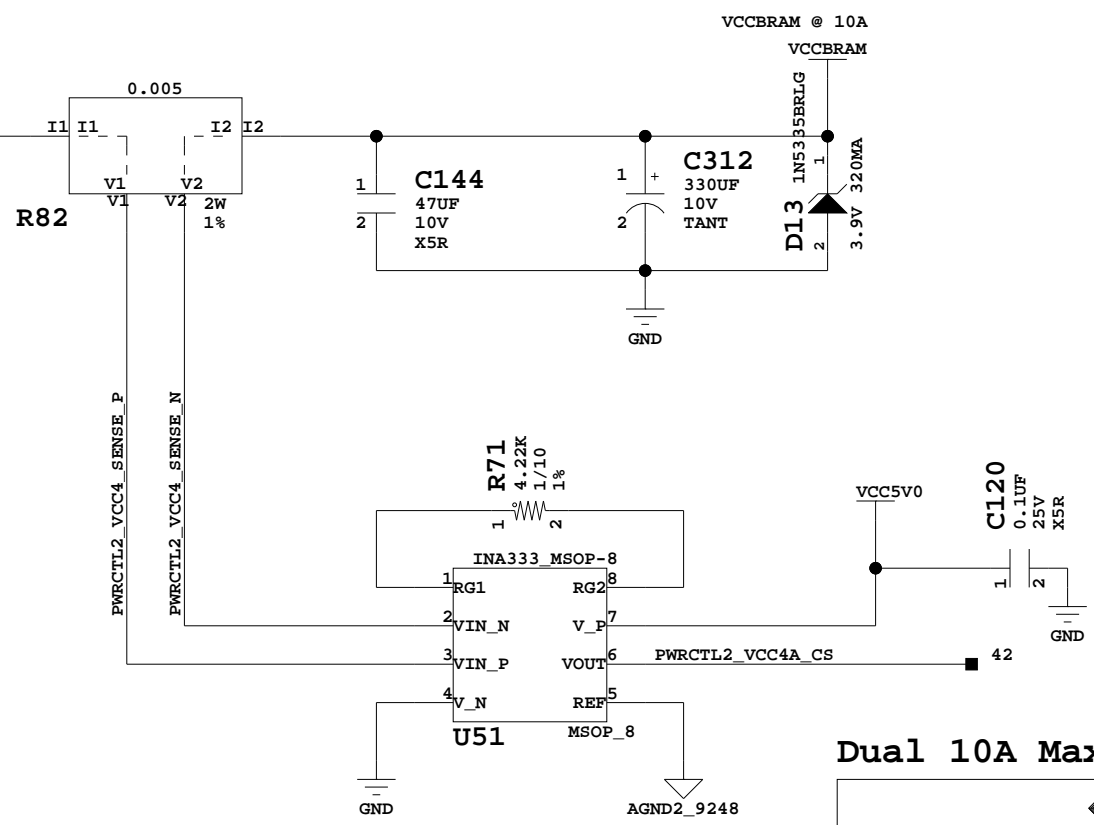
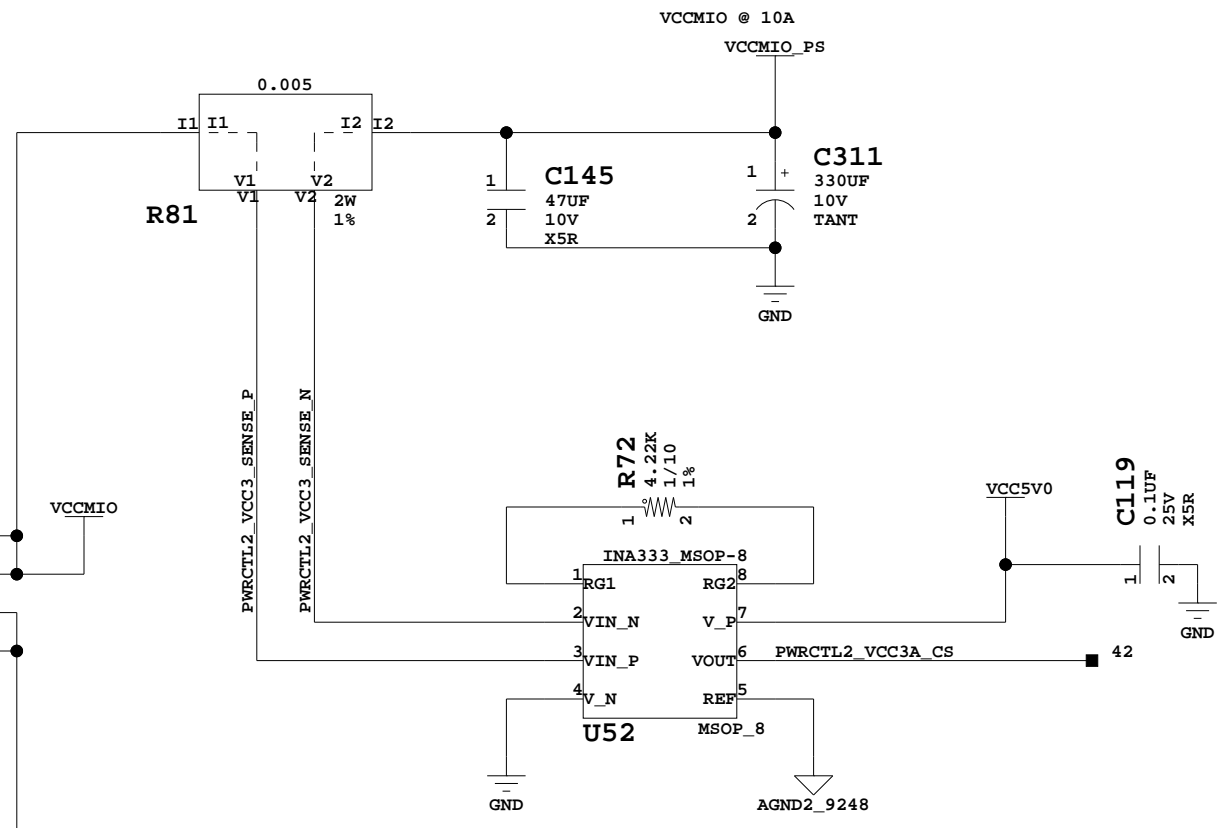
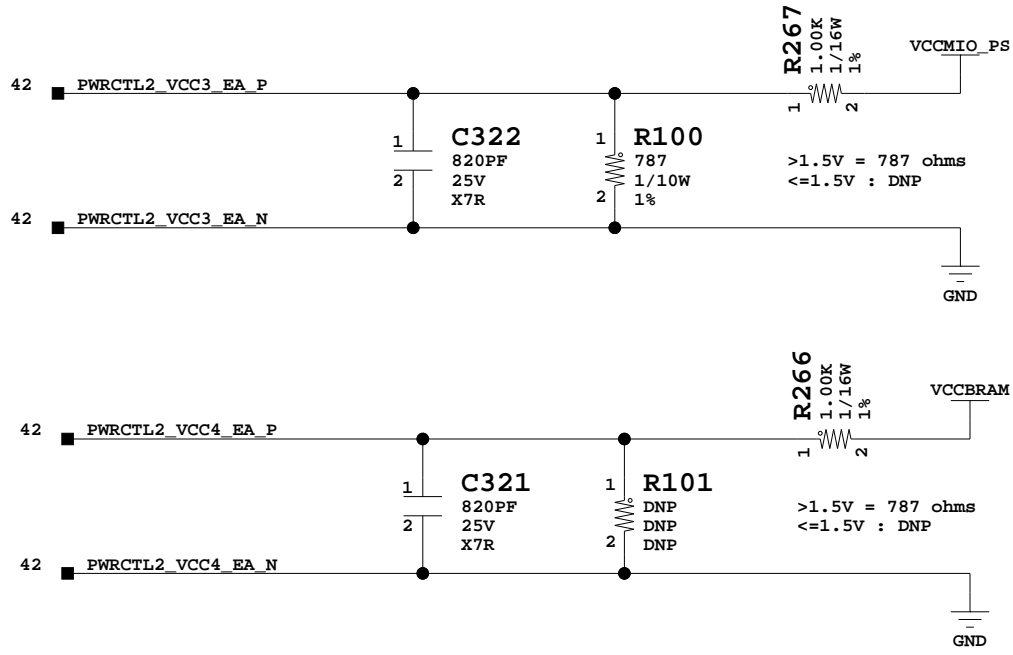
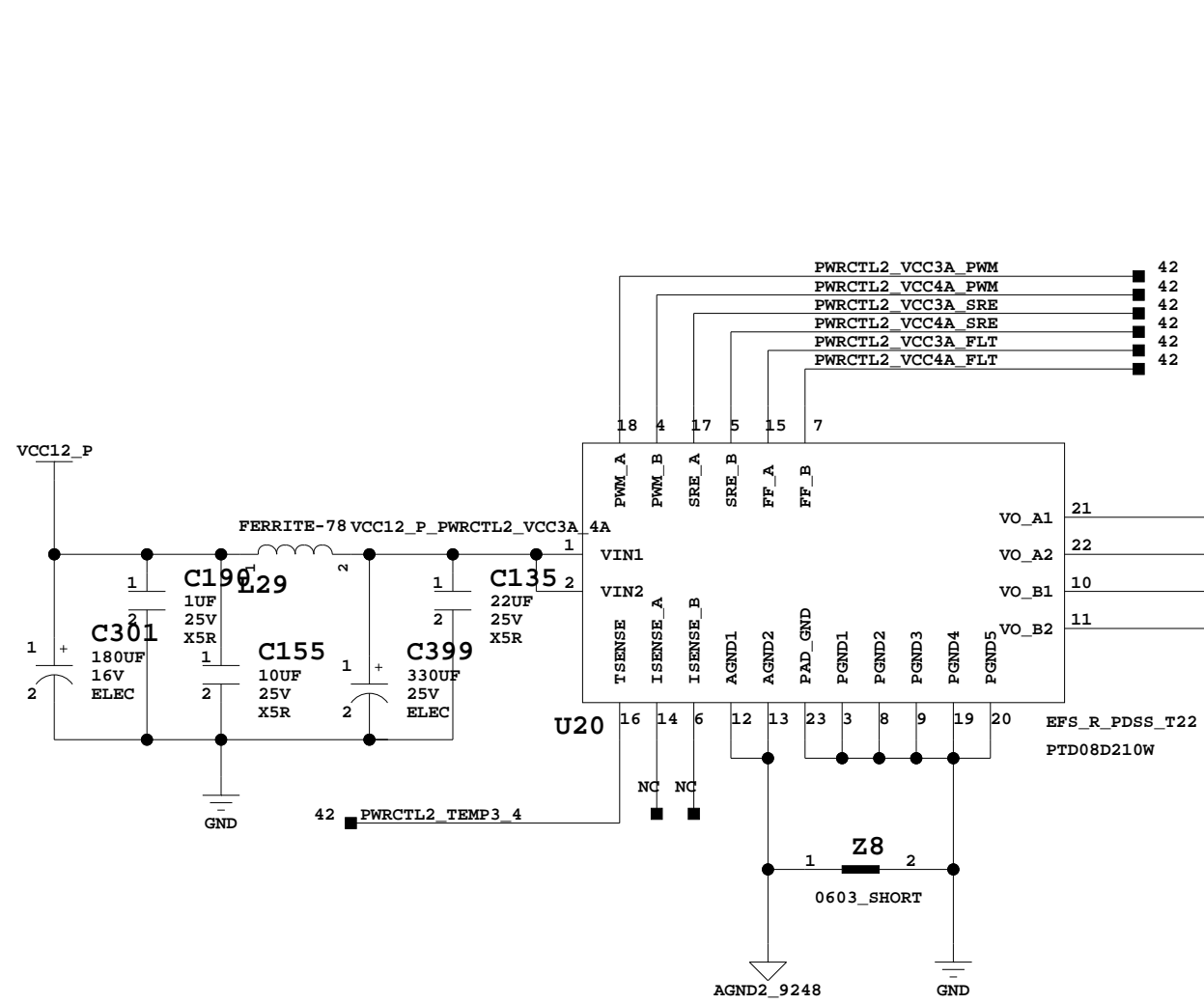
- 39, 45, 47 PMBUS_ALERT 35
- 32, 39, 45, 47 PMBUS_DATA 20
- 32, 39, 45, 47 PMBUS_CLK 19
- 39, 45, 47 PMBUS_CTRL 36
- 42 PWRCTL2_TMUX0 39
- 42 PWRCTL2_TMUX1 40
- 42 PWRCTL2_TMUX2 54
- 42 PWRCTL2_TEMP 7

PMBUS Addr = 53



Dual 10A Max. Power Channels

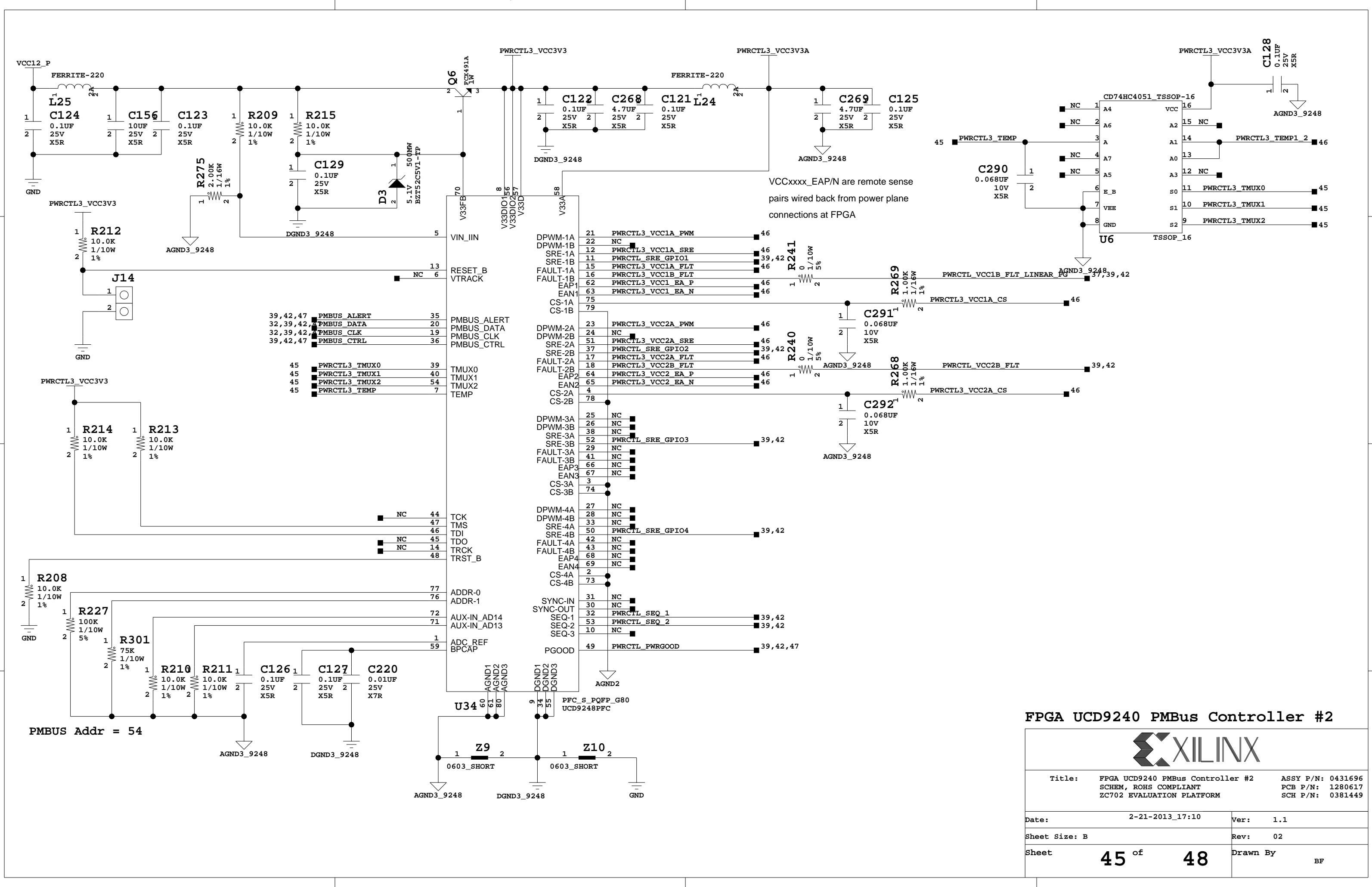
Title: Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 43 of 48	Drawn By BF	



Dual 10A Max. Power Channels



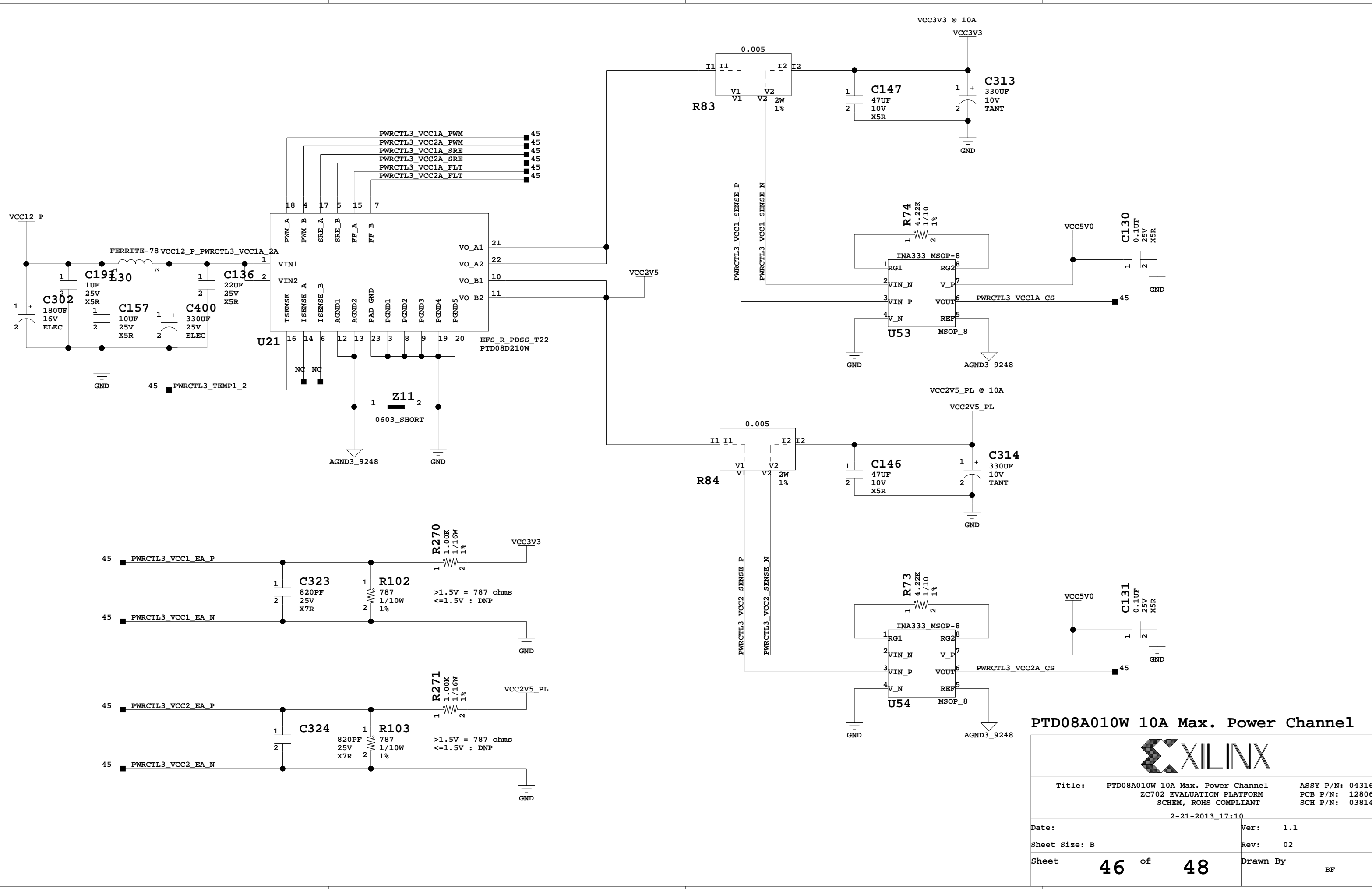
Title: Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 44 of 48	Drawn By	BF



FPGA UCD9240 PMBus Controller #2



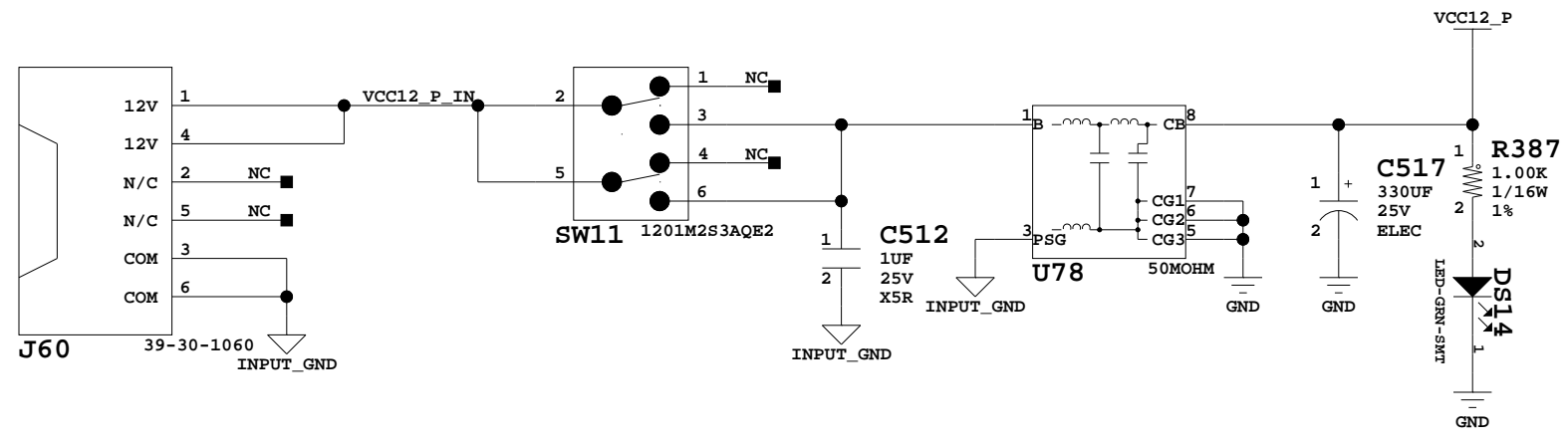
Title: FPGA UCD9240 PMBus Controller #2		ASSY P/N: 0431696
SCHEM, ROHS COMPLIANT		PCB P/N: 1280617
ZC702 EVALUATION PLATFORM		SCH P/N: 0381449
Date: 2-21-2013_17:10	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 45 of 48	Drawn By	BF



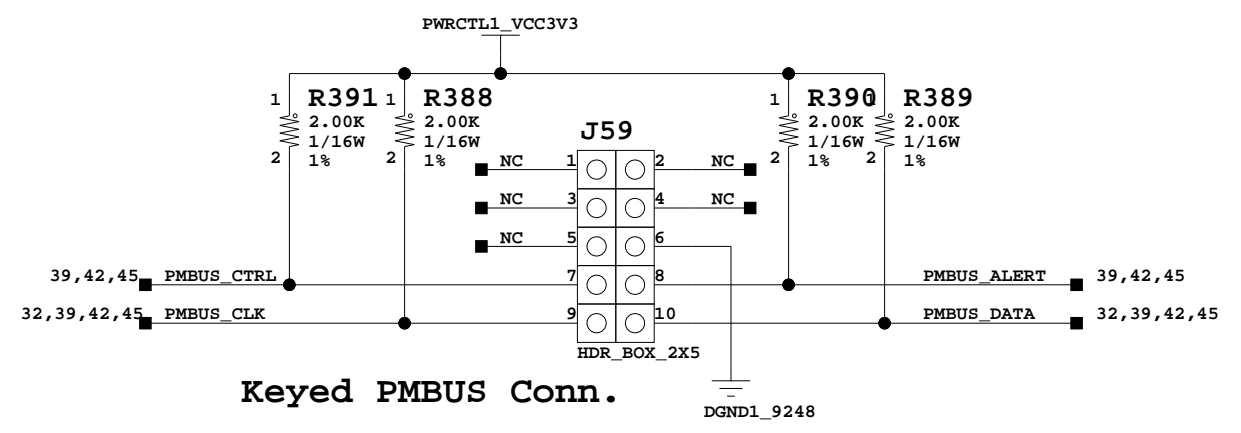
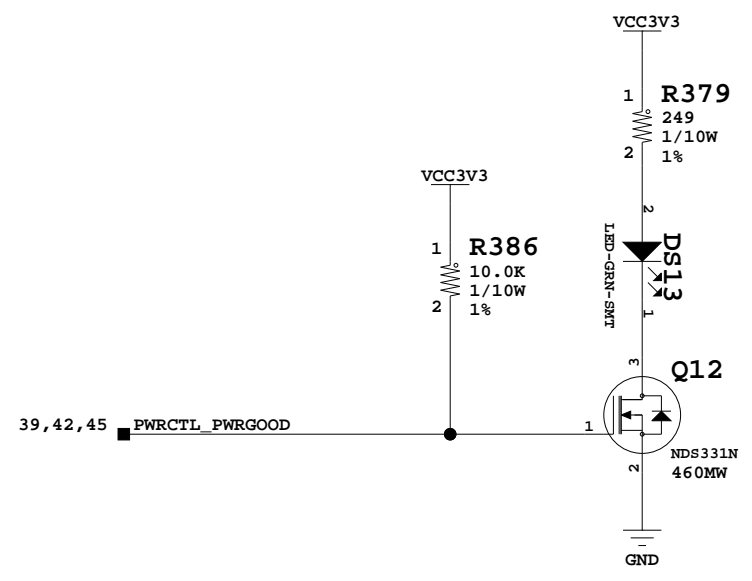
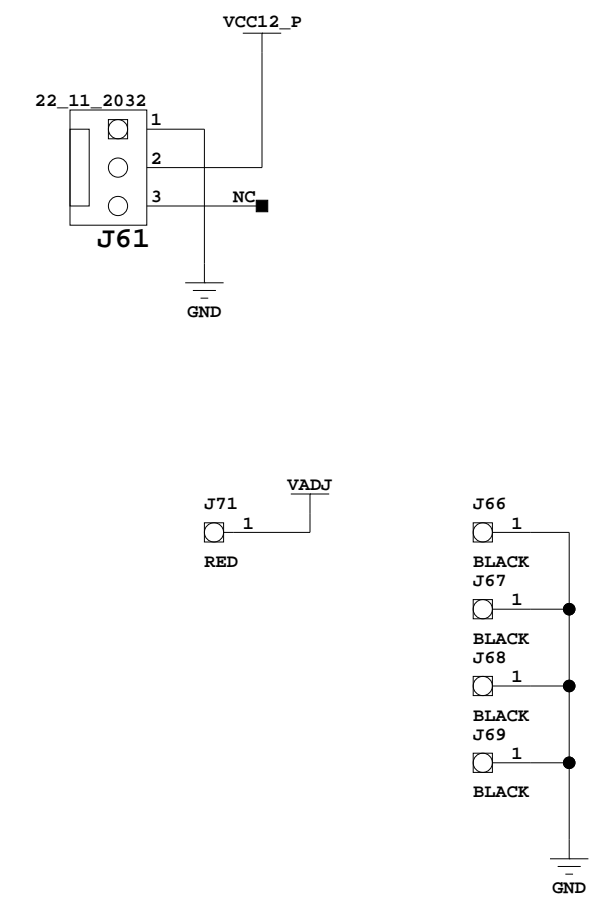
PTD08A010W 10A Max. Power Channel

Title: PTD08A010W 10A Max. Power Channel ASSY P/N: 0431696
 ZC702 EVALUATION PLATFORM PCB P/N: 1280617
 SCHEM, ROHS COMPLIANT SCH P/N: 0381449
 2-21-2013 17:10

Date: Ver: 1.1
 Sheet Size: B Rev: 02
 Sheet **46** of **48** Drawn By BF

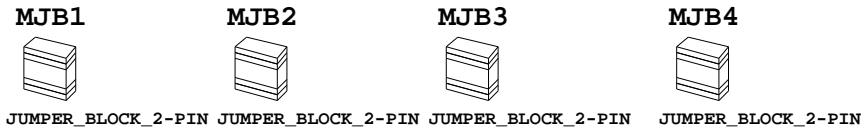
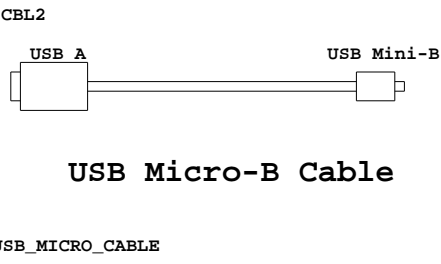
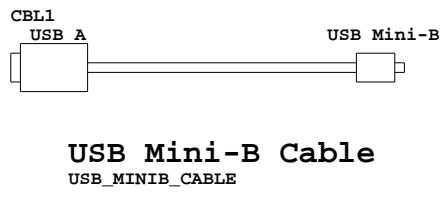
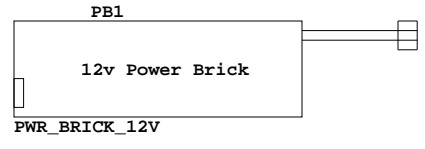
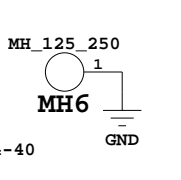
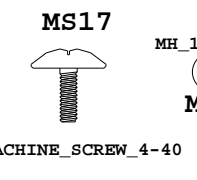
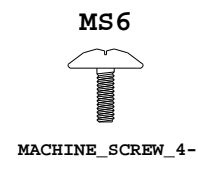
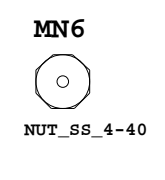
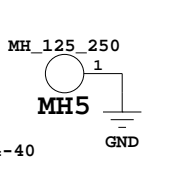
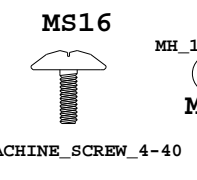
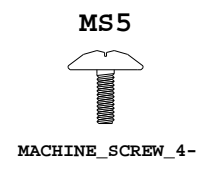
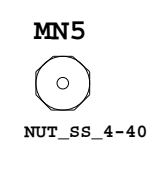
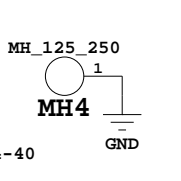
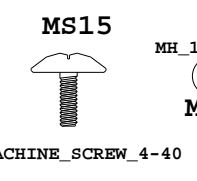
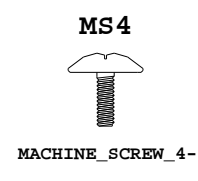
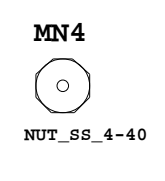
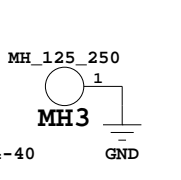
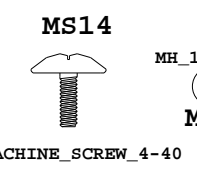
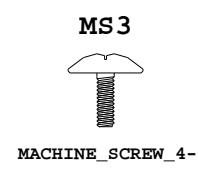
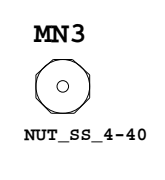
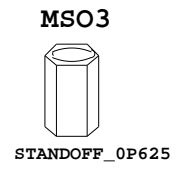
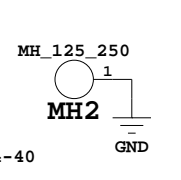
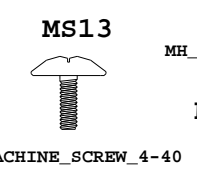
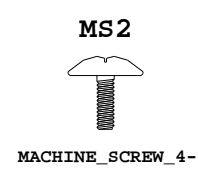
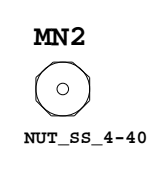
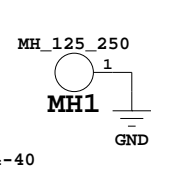
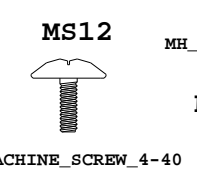
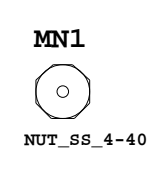
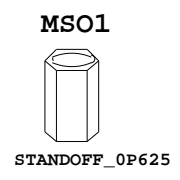


Keyed Fan Header



Power Connector and switch, PMBus Header

Title: Power Connector and switch, PMBus Header ASSY P/N: 0431696 SCHEM, ROHS COMPLIANT PCB P/N: 1280617 ZC702 EVALUATION PLATFORM SCH P/N: 0381449	
Date: 2-21-2013_17:10	Ver: 1.1
Sheet Size: B	Rev: 02
Sheet 47 of 48	Drawn By BF



Mechanical Components

<p>Title: Mechanical Components SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM</p>	
<p>ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449</p>	
Date: 2-21-2013_17:10	Ver: 1.1
Sheet Size: B	Rev: 02
Sheet 48 of 48	Drawn By BF